Howard W. Sams PUBLICATION

21200

DIGITAL EQUIPMENT SERVICING GUIDE

By
Robert G. Middleton

Digital Equipment Servicing Guide

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HOWARD W. SAMS & CO., INC.
THE BOBBS-MERRILL CO., INC.
INDIANAPOLIS · KANSAS CITY · NEW YORK

FIRST EDITION

FIRST PRINTING—1975

International Standard Book Number: 0-672-21200-5
Library of Congress Catalog Card Number: 75-5411

Preface

Technicians who have had experience in troubleshooting only linear electronic circuitry, such as tv receivers, may believe that digital circuitry is formidably complex. Although digital circuitry *is* different, it is not true that troubleshooting procedures are unusually difficult. There is nothing really novel or exotic in digital equipment. The chief requirement is to learn how to "think digital"—in other words, to reason in terms of switching circuitry. Initial clues come chiefly from symptoms of malfunction. These symptoms are then evaluated with respect to both the block diagram and the schematic diagram for the digital equipment. In turn, the sections or circuits that fall under suspicion are checked out by means of dc voltage measurements, continuity tests, scope waveforms, or specialized digital test equipment such as logic probes, pulsers, and clips. In the case of modular construction, quick checks may be made by simply plugging in a replacement module.

This book starts at the beginning and guides the technician up to comparatively sophisticated digital frequency display equipment. Digital servicing is one of the areas in which there is no real substitute for practical "hands-on" experience. Accordingly, the reader is strongly advised to construct and test the basic flip-flops, gates, and digital assemblies described in the early chapters. Topics covered are basic digital technology, digital logic gates, binary adders, subtracters, bcd counters, gates and associated equipment, display devices and operation, digital logic in electronic instruments, and digital frequency display equipment. Binary arithmetic and digital logic laws are introduced only to the extent that is actually required for practical servicing procedures.

One of the stumbling blocks for the apprentice digital technician is digital terminology, which is different from linear terminology. Therefore, technical terms are carefully explained throughout the book and are supplemented by practical illustrations. It is my firm belief and sincerest hope that this book will be a valuable addition to the libraries of all present and future technicians, as well as to technical-school programs.

ROBERT G. MIDDLETON

Contents

CHAPTER 1

Basic Digital Technology

Digital technology is concerned with electronic systems that use switching circuits. In other words, a digital circuit is either "on" or it is "off." A digit is a number, and a digital circuit is either in the "1" state or it is in the "0" state. Digital circuits are utilized primarily in electronic computers. However, the technician also encounters digital circuits in test instruments such as digital voltmeters (DVM's), in digital communication systems, in digital clocks, in white-dot/crosshatch/color-bar generators, in tv remote-control units, in various amusement coin machines, and in many other applications as described in following chapters. Almost all modern digital circuits employ semiconductor devices.

Common trouble symptoms caused by defects in digital systems are as follows:

1. No output.
2. Incorrect output.
3. Occasional incorrect output.
4. Intermittent operations.

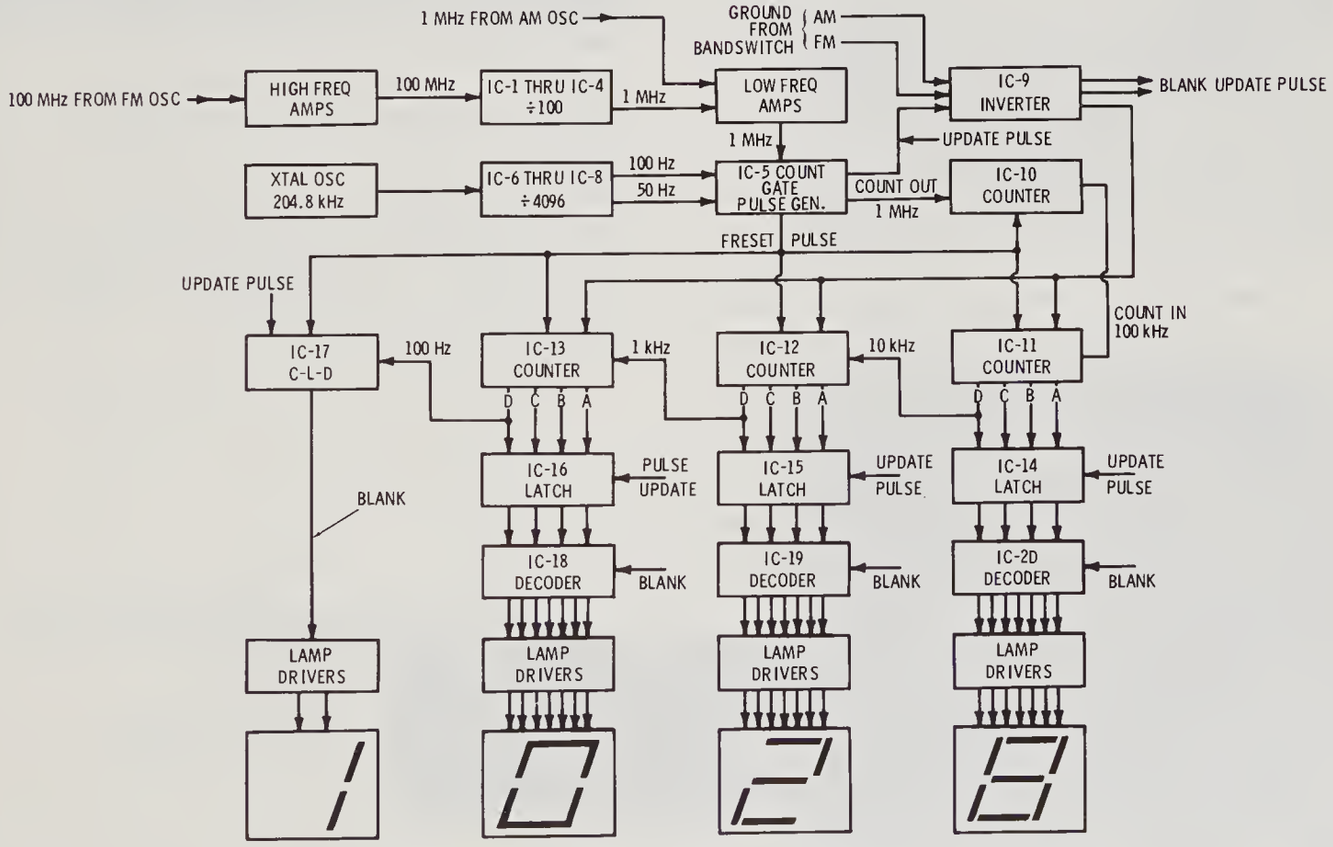


Fig. 1-1. Block diagram of a digital tuning indicator display arrangement.

5. "Stuck at" readout.
6. Missing numeral(s) in readout.
7. "Freewheeling" operation in absence of input.

GENERAL DISCUSSION

A block diagram of a digital tuning indicator (dti) is shown in Fig. 1-1. Although the dti system appears to be very complicated, most digital-circuit functions can be classified in one of the following categories:

1. Flip-flops.
2. Gates.
3. Pulse generators.

Digital logic sets forth rules or laws for operation of switching circuits that add, subtract, multiply, and divide, and so on. Some digital-logic systems perform highly complex operations in advanced mathematics used by engineers and scientists. Flip-flops, gates, and pulse generators may be manufactured with discrete components on circuit boards, as shown in Fig. 1-2. This is an example of a pulse generator. Note that this circuit board has been physically damaged and its corner is broken as indicated by the arrow. Most digital circuit boards are manufactured with integrated circuits, as exemplified in Fig. 1-3. This is an example of a plug-in circuit board, or *module*. It is easier to understand discrete-component circuits than integrated circuits. Therefore, we will examine the basic discrete-component digital circuit configurations at this time, and then return to integrated circuitry in a following chapter. You should construct and test the configurations described in this chapter in order to learn what you need to know as fast and as efficiently as possible.

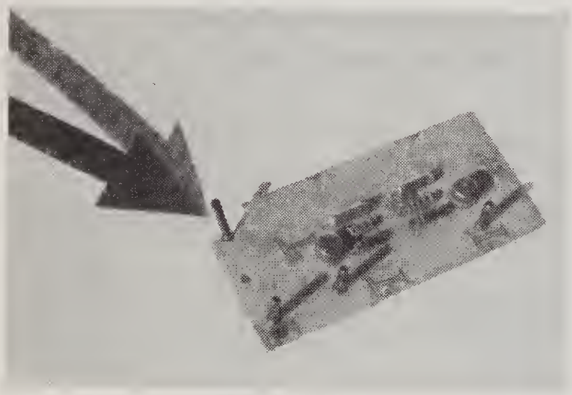


Fig. 1-2. A pulse generator with discrete components showing an example of physical damage.

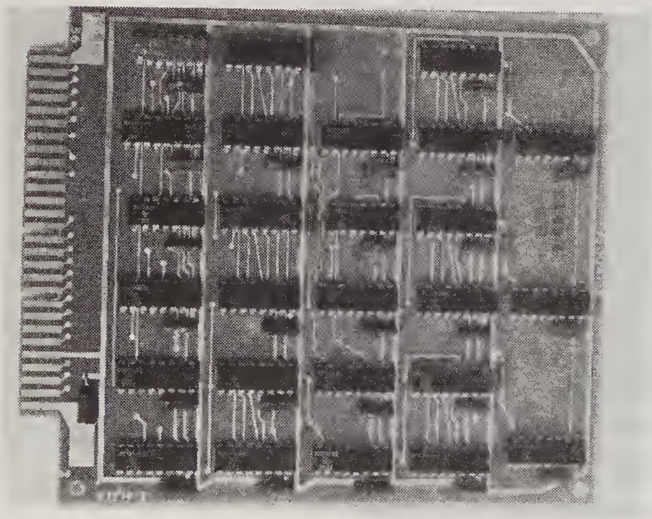
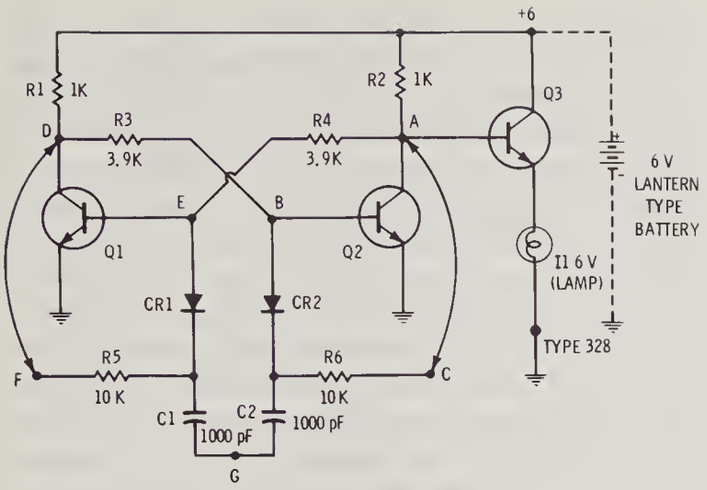


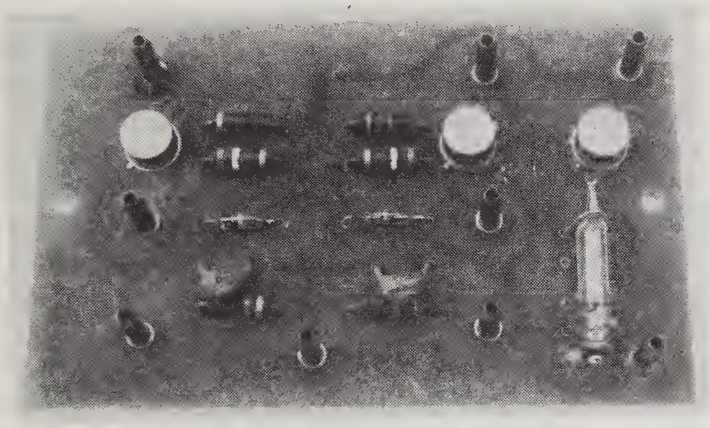
Fig. 1-3. A digital-circuit module employing integrated circuits.

BASIC FLIP-FLOP ARRANGEMENT

A flip-flop (FF) is also called a bistable multivibrator, Eccles-Jordan circuit, or trigger circuit. Fig. 1-4 shows a basic flip-flop configuration and a typical flip-flop circuit board with discrete components. Observe that transistor Q3 is a switch which causes lamp I1 to glow when Q3 is conducting. At this point in your experiments, connect terminal D to F, and connect terminal A to C. Later on, these terminals will be connected to other units. Note that when you first connect the 6-volt battery to the flip-flop, the lamp may or may not glow. This depends on the particular circuit tolerances. If the lamp is not glowing, it can be turned on by short-circuiting terminal D to terminal E temporarily. Or, if the lamp is glowing, it can be turned off by short-circuiting terminal A to terminal B temporarily. These responses are obtained because the three transistors must be in one of the following states:



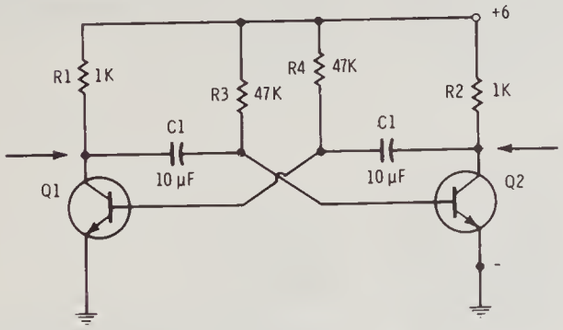
(A) Configuration.



Courtesy, LIBE Co.

(B) Circuit board.

Fig. 1-4. Basic flip-flop arrangement



(A) Circuit.

(B) Output waveform.

Courtesy, LIBE Co.

Fig. 1-5. Pulse (square-wave) generator.

	Q1	*Q2*	*Q3*
Lamp "on"	on	off	on
Lamp "off"	off	on	off

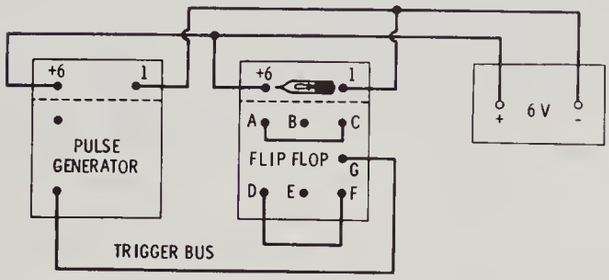
Unless there is a component defect in the circuit board, the foregoing conditions are the only two possible states of the flip-flop. It is instructive to measure the collector voltages of the transistors in their two states. Note that if Q1 is conducting, its collector voltage is almost zero. On the other hand, if Q1 is not conducting, its collector voltage is approximately 5 volts. The same collector-voltage relationships will be found for Q2. However, the collector voltage of transistor Q3 is 6 volts, whether the lamp is on or off. The reason for this is that the collector of Q3 is directly connected to the 6-volt battery.

PULSE GENERATOR

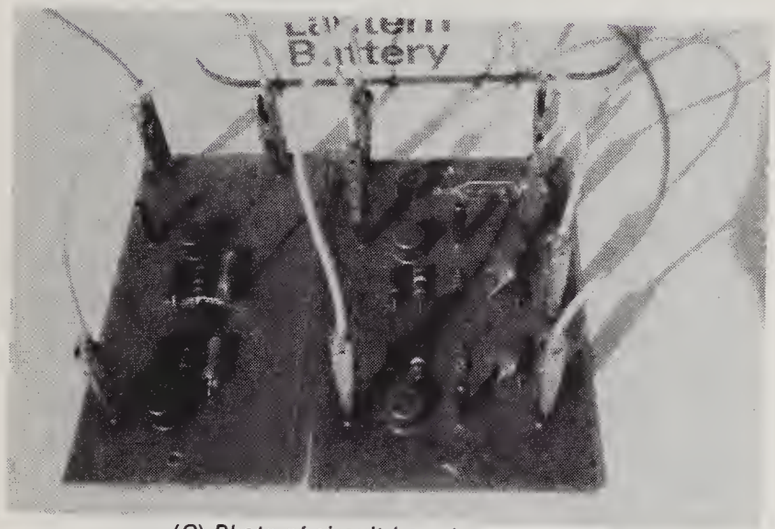
A pulse generator was illustrated in Fig. 1-2. This is actually a square-wave generator. However, when its square-wave output is differentiated, a train of pulses is produced. The pulse-generator circuit is shown in Fig. 1-5. It is an astable (free-running) multivibrator with a repetition rate of approximately two pulses per second (pps). Higher repetition rates will be obtained if the values of the coupling capacitors (C1) are reduced. It is instructive to employ a low repetition rate at this time so that digital circuit actions can be observed directly. The amplitude of the square-wave output shown in Fig. 1-5B is approximately 6 volts peak to peak (p-p). Note that the output can be taken from the collector of either Q1 or Q2. The only difference between these two output waveforms is that they are 180° out of phase, or one waveform will be positive-going while the other waveform is negative-going.

A pulse generator is also called a clock; it is the primary source of synchronizing pulses in an electronic computer. Consider a pulse generator triggering a flip-flop, as depicted in Fig. 1-6. The

(A) Block diagram.



(B) Detailed block diagram.



(C) Photo of circuit-board arrangement.

Fig. 1-6. Flip-flop driven by a pulse generator.

circuitry for this arrangement is shown in Fig. 1-7. The square-wave output from the pulse generator is differentiated by C1 and C2 in the flip-flop. In turn, triggering takes place by means of spike waveforms, as seen in Fig. 1-8. Observe that diodes CR1 and CR2 will permit only negative pulses to pass. Note also that when Q1 is cut off, CR1 is reverse-biased about 5 volts but CR2 is practically zero-biased. On the other hand, when Q2 is cut off, CR2 is reverse-biased about 5 volts but CR1 is practically zero-biased. Therefore, when a negative trigger pulse arrives, it can pass only through the zero-biased diode. For example, if Q1 is cut off, the trigger pulse passes through CR2 and cuts off Q2 momentarily. As a result, Q1 is driven into conduction, and the flip-flop changes state. The following trigger pulse will be applied to Q1 through CR1, and the flip-flop will change state again. CR1 and CR2 are called steering diodes because they steer the trigger pulse to the conducting transistor. If A is not connected to C, and D is not connected to F, the flip-flop will not trigger because the pulse is then applied to the bases of both transistors, which prevents the nonconducting transistor from being driven into conduction.

Single-shot triggering is depicted in Fig. 1-9. A 0.05-μF capacitor is used as a single-shot pulse source. First, the capacitor is charged by touching its terminals to a 6-volt battery. The flip-flop can then be triggered as shown in the diagram. If the capacitor is then recharged, the flip-flop can be triggered once more. Single-shot triggering often provides a useful method of trouble analysis in digital systems.

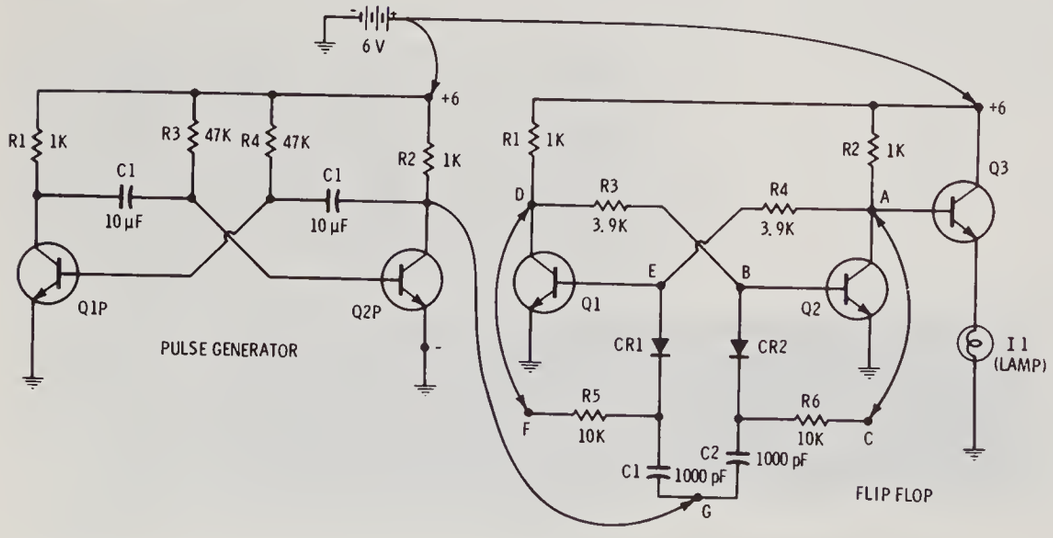
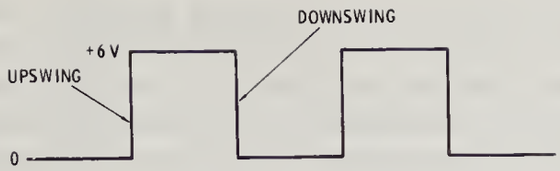
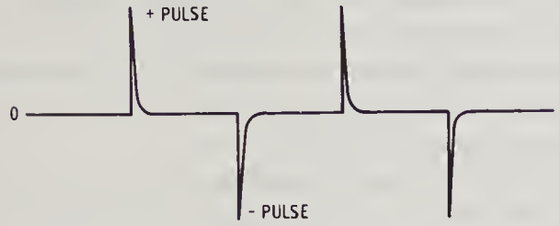


Fig. 1-7. Schematic diagram of the arrangement shown in Fig. 1-6.

Courtesy, LIBE Co.



(A) Output from pulse generator.



(B) Differentiated waveform that triggers the flip-flop.

Fig. 1-8. Pulse generator waveforms.

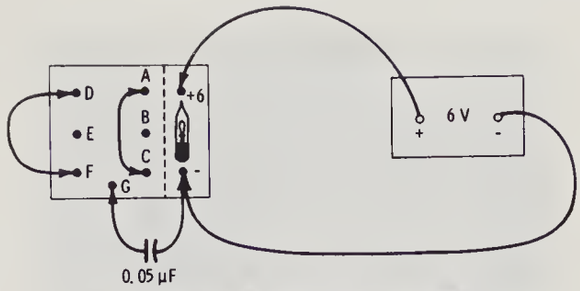
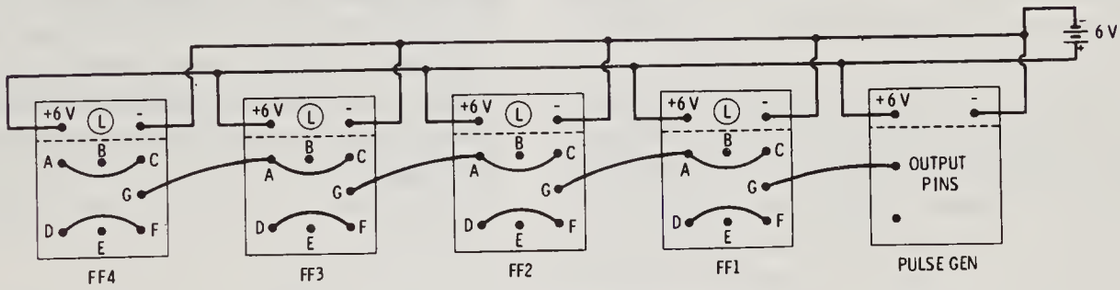


Fig. 1-9. Single-shot triggering of flip-flop.

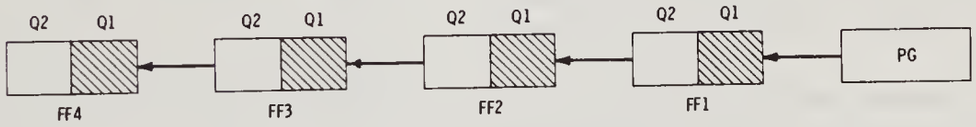
BINARY-UP COUNTER

Next, consider the binary-up counter shown in Fig. 1-10. This arrangement counts up to 16 pulses and then starts over again. It consists of four flip-flops, which are triggered in turn. Pulses

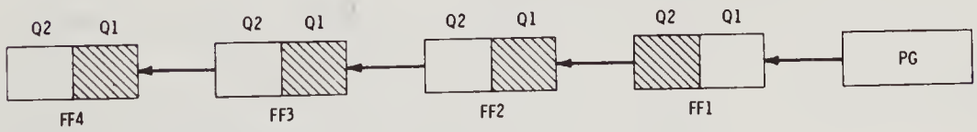
(A) Block diagram.



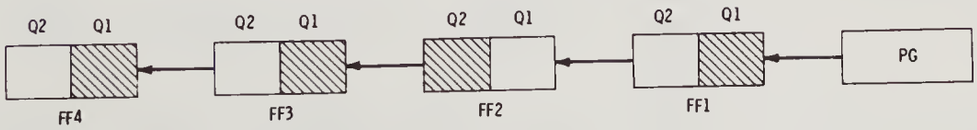
(B) Circuit-board interconnections.



(C) Flip-flop states before first pulse is applied.



(D) Flip-flop states after first pulse is applied.



(E) Flip-flop states after second pulse is applied.

Fig. 1-10. Binary-up counter arrangement.

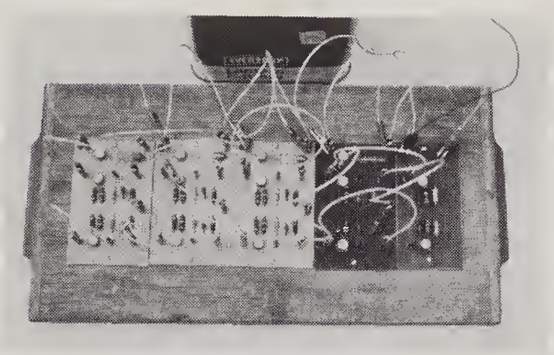


Fig. 1-11. An experimental binary-up counter with flip-flops.

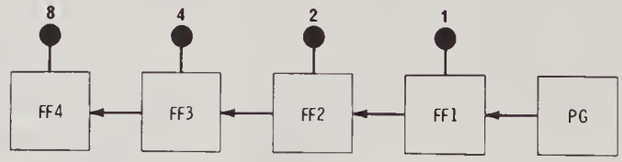
are applied to the first flip-flop by a pulse generator. The flip-flop circuit is shown in Fig. 1-4, and the pulse-generator circuit is shown in Fig. 1-5. Before the first pulse is applied, the flip-flop transistors are in the states depicted in Fig. 1-10C. In turn, all of the flip-flop lamps are dark. Next, when a pulse is applied to FF1, it changes state and its lamp glows; this change in state is shown in Fig. 1-10D. Again, when a second pulse is applied to FF1, it changes back to its original state and, in so doing, triggers FF2. These changes in state are depicted in Fig. 1-10E. Now, the FF2 lamp glows and the FF1 lamp extinguishes. If following pulses are applied to FF1, the chain process continues until the FF4 lamp glows. Then, the next pulse causes all the lamps to extinguish, and the process starts over again.

A photograph of the counter arrangement in Fig. 1-10 is shown in Fig. 1-11. This is called a 4-*bit* counter. Bit is an abbreviation for binary digit. It designates one of two possible states, such as the on and off states of a flip-flop indicator lamp. These on and off states correspond to the binary numbers 1 and 0. In other words, the binary number 1 corresponds to *on* and the binary number 0 corresponds to *off*. In the binary system, which is used almost exclusively in digital computers, there are only two digits: 1 and 0. Binary arithmetic is simpler than ordinary decimal arithmetic. However, binary arithmetic seems difficult on first acquaintance because we are not familiar with reading binary numbers. It is instructive to consider a few numbers shown in both binary and decimal form in Table 1-1.

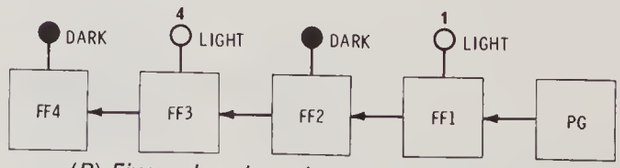
The easiest way to read out a binary-up counter is to assign decimal numbers to each flip-flop, as shown in Fig. 1-12A. Thus, the first FF has a decimal value of 1, the second FF has a decimal value of 2, the third FF has a decimal value of 4, and the fourth FF has a decimal value of 8. In turn, if the first and third FF indicator lamps are on, as depicted in Fig. 1-12B, a count of 4 + 1, or 5, is indicated. If the third and fourth FF lamps are on, as shown in Fig. 1-12C, a count of 8 + 4, or 12, is indicated. Referring to Table 1-1, it is evident that after 15 pulses have been applied, the counter will have all four indicator lamps on. After 16 pulses have been applied, all of the lamps go off. Then the counter starts all over again.

Table 1-1. Decimal-Binary Equivalents

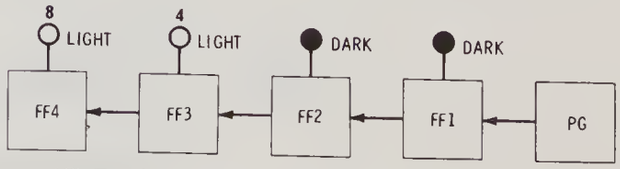
Decimal	Binary
0	0
1	1
2	10
3	11
4	100
5	101
6	110
7	111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101
14	1110
15	1111



(A) Decimal numbers are assigned to the flip-flops.



(B) Five pulses have been counted (4 + 1).



(C) Twelve pulses have been counted (8 + 4).

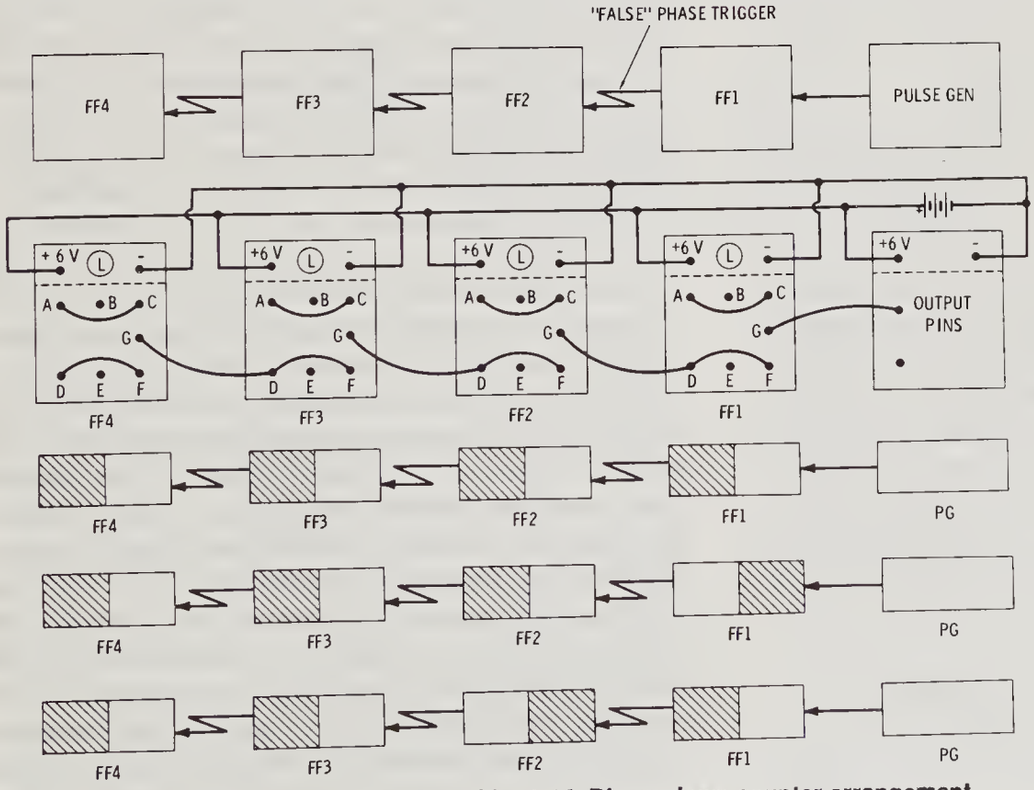
Fig. 1-12. Reading a binary-up counter.

When you first apply power to the binary-up counter, you will note that the indicator lamps may be either on or off in an unpredictable order. The state of the lamps depends entirely upon the component tolerances in the flip-flop circuits. Accordingly, an arbitrary readout number is displayed at this time. After you start up the pulse generator, this arbitrary number increases with each applied pulse until all the lamps are on. Then, all the lamps go out and the counter starts counting from 1 up to 15, whereupon all the lamps go out again. The counter automatically runs out to a 0-0-0-0 display, no matter what the arbitrary starting number might be. Note that a binary-up counter operates as a sequential adder. In other words, it indicates the sum of the pulses in a train. The counter is also a memory, in that it will store a binary number indefinitely.

Troubleshooting a malfunctioning flip-flop can often be done on the basis of comparative resistance measurements. For example, if the indicator lamp does not respond when the flip-flop is triggered, it is possible that the lamp filament is burned out. To check this possibility, an ohmmeter may be used to measure the resistance across the terminals of lamp I1 in Fig. 1-7. Such measurements can be made to best advantage with a hi-lo ohmmeter, such as shown in Fig. 1-13. This instrument applies less than 0.1 volt between the points under test and cannot "turn on" a normal transistor or diode. Comparative resistance measurements involve ohmmeter checks between corresponding terminal points of malfunctioning

Courtesy, Sencore

Fig. 1-13. A FET meter with hi-lo ohmmeter functions.



(A) Block diagram.

(B) Circuit-board interconnections.

(C) Flip-flop states before first pulse is applied.

(D) Flip-flop states after first pulse is applied.

(E) Flip-flop states after second pulse is applied.

Fig. 1-14. Binary-down counter arrangement.

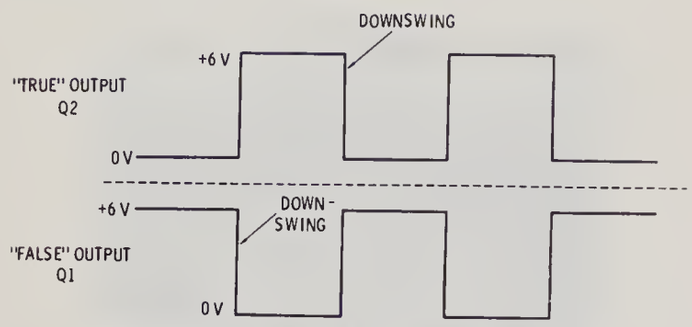


Fig. 1-15. "True" and "false" outputs from a flip-flop.

circuit boards and similar known-good circuit boards.

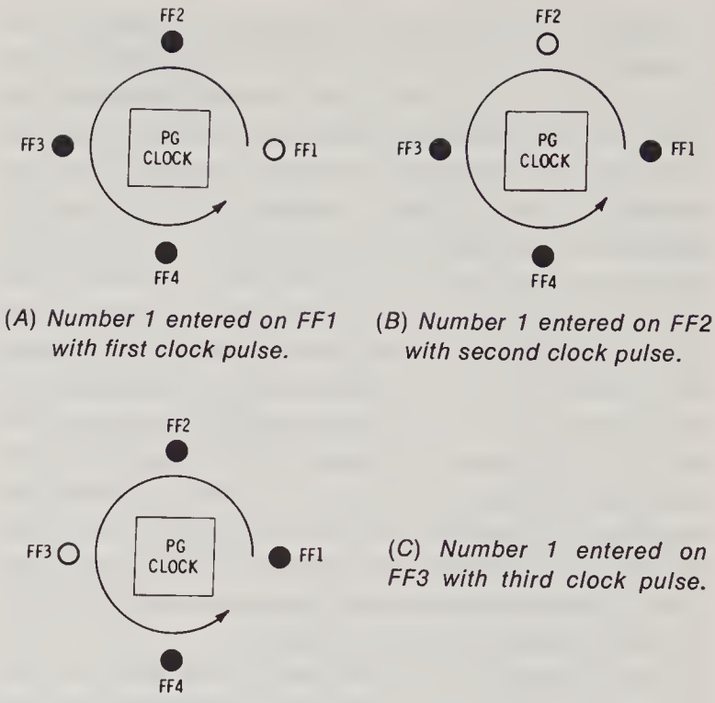
BINARY-DOWN COUNTER

By means of a slight rearrangement of trigger leads, a binary-up counter can be changed over into a binary-down counter, as shown in Fig. 1-14. A "down" counter operates the same as an "up" counter except that it counts backwards, starting from the maximum display capability. As an example, if four flip-flops are employed, the down counter indicates the sequence 15, 14, 13, 12, 11, 10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0, and then starts over again. The reason a countdown is obtained is that each flip-flop triggers the next flip-flop by means of an output waveform which is 180° out of phase with the trigger waveform employed in an up counter. We will utilize both up and down counters in more-elaborate digital arrangements such as adders.

Referring to Fig. 1-15, observe the output waveforms from the flip-flops. When the lamp is on, transistor Q2 in Fig. 1-4 provides the "true" output at its collector, whereas transistor Q1 provides the "false" output at its collector. These true and false waveforms are 180° out of phase with each other. As explained previously, one flip-flop can trigger a succeeding flip-flop only on the downswing (negative-going) interval of its output waveform. Since downswings are produced by Q2 when it goes into conduction, and downswings are produced by Q1 when Q2 goes into cutoff, the difference in triggering sequences between an up counter and a down counter is apparent. (Compare Fig. 1-10 with Fig. 1-14.)

BINARY LEFT-SHIFT REGISTER

A binary left-shift register will shift any binary number to the left after it has been entered,



(A) Number 1 entered on FF1 with first clock pulse.

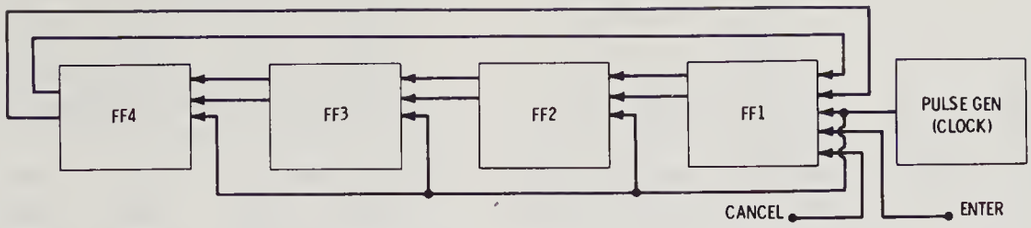
(B) Number 1 entered on FF2 with second clock pulse.

(C) Number 1 entered on FF3 with third clock pulse.

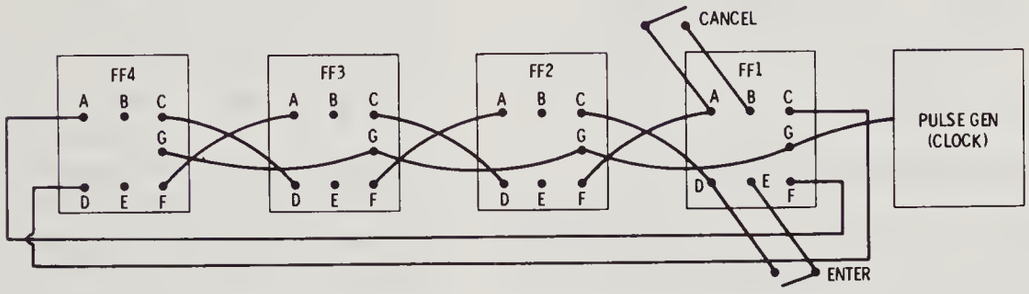
Fig. 1-16. Principle of binary shift register.

and then do an "end-around" shift from the last flip-flop to the first. The easiest way to understand a shift register is to consider that it is a circle of flip-flops, as depicted in Fig. 1-16. In this example, the binary number 1 has been entered on FF1. An entry can be made only during the occurrence of a pulse (clock pulse) from the pulse generator. On the next clock pulse, the FF1 lamp stops glowing and the FF2 lamp starts glowing. In other words, the binary number 1 has been shifted one place. Then, on the succeeding clock pulse, the FF2 lamp stops glowing and the FF3 lamp starts glowing. Thus, the binary number 1 has been shifted another place. The process will continue indefinitely, and the glowing lamp will keep shifting until the binary number has been cancelled.

Referring to Fig. 1-17A we observe a block diagram for a 4-bit binary left-shift register. The pulse generator in this arrangement is generally called a clock. The corresponding circuit-board interconnections are shown in Fig. 1-17B. Observe that a switch is used to enter a binary number and another is used to cancel the binary number. With reference to the circuit diagram in Fig. 1-4, observe that an entry is made by momentarily shortcircuiting the collector to the base of Q1, and that a cancellation is made by momentarily shortcircuiting the collector the base of Q2. In other words, if lamp I1 is not glowing, the lamp will start to glow when Q1 is thrown into conduction.

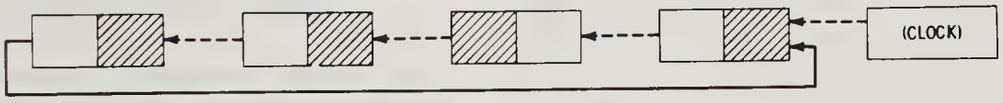


(A) Block diagram.

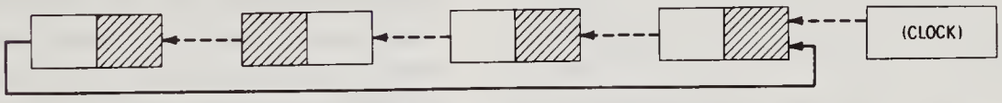


(B) Circuit-board interconnections (battery connections omitted).

(C) Number 1 entered on FF1 with first clock pulse.



(D) Number moved to FF2 with second clock pulse.



(E) Number moved to FF3 with third clock pulse.

Fig. 1-17. Binary left-shift register arrangement.

Or, if lamp I1 is glowing, the lamp will stop glowing when Q2 is thrown into conduction.

Suppose that all four lamps in Fig. 1-17B are dark. In this case, there is no binary number entered, and the lamps will remain dark although the pulse generator (clock) is operating. Now, if the "enter" switch is momentarily closed while a clock pulse is applied, the FF1 lamp starts glowing. This is the situation shown in Fig. 1-17C. On the next clock pulse, the FF1 lamp turns off and the FF2 lamp turns on, as depicted in Fig. 1-17D. Again, on the succeeding clock pulse, the FF2 lamp turns off and the FF3 lamp turns on, as shown in Fig. 1-17E. Finally, a shift occurs from FF4 back to FF1, and the process continues until the binary number is cancelled. Cancellation is accomplished by momentarily closing the "cancel" switch while the FF1 lamp is glowing and a clock pulse is occuring. Then, all the lamps will be dark.

Next, suppose that we start with all of the lamps dark and that we enter the binary number 1 four times in succession. In such a case, the shift register will display the binary number 1111 (decimal number 15); in other words, all four lamps will glow continuously until part or all of the entered number is cancelled. This shift register uses the JK flip-flop configuration to obtain the operating sequence described in the preceding paragraph. A JK flip-flop configuration is shown in Fig. 1-18. You will meet this arrangement over

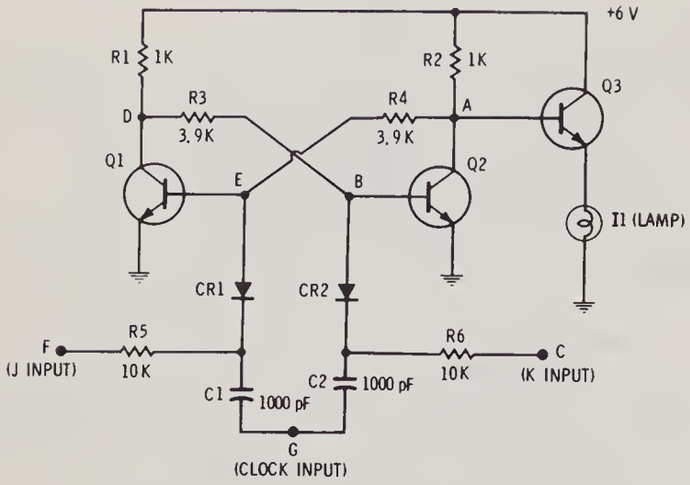
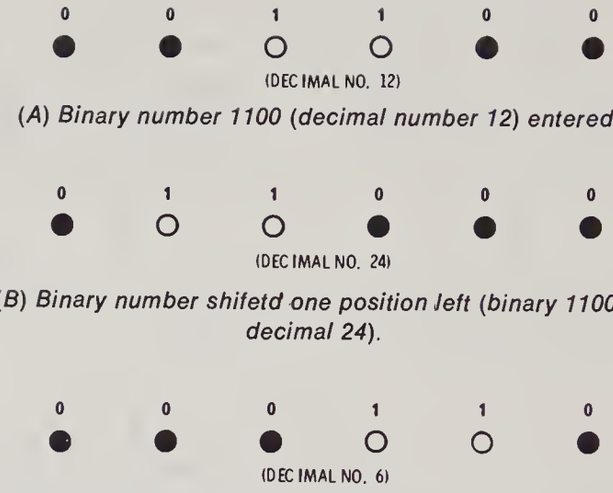


Fig. 1-18. Configuration of a JK flip-flop.



(A) Binary number 1100 (decimal number 12) entered.

(B) Binary number shifetd one position left (binary 11000, decimal 24).

(C) Entered binary number shifted one position right (binary 110, decimal 6).

Fig. 1-20. Change in numerical value with shift.

and over again in computer systems. Note that the JK circuit is the same as the flip-flop in Fig. 1-4, except that terminal F is not connected to terminal D, and terminal C is not connected to terminal A. Instead, separate inputs are applied to terminals C and F. These are called the J input and the K input. The J input may be positive or zero—either +6 volts or zero volts approximately. Similarly, the K input may be positive or zero. The clock pulse is applied at terminal G. Note that a clock pulse cannot trigger the flip-flop unless suitable J and K inputs are present.

Consider the circuit action that occurs in Fig. 1-18. Suppose that a positive voltage is applied to the J input. As a result, diode CR1 is reverse-biased, or "held off." Accordingly, a negative trigger pulse cannot flow through CR1 to the base of Q1. In other words, transistor Q1 cannot be turned off if it is already conducting. However, the negative trigger pulse can flow through CR2 and turn Q2 off if it is already conducting. Next, suppose that a positive voltage is applied to the K input; in turn, CR2 is reverse-biased, or "held off." Accordingly, a negative trigger pulse cannot flow through CR2 to the base of Q2. In other words, Q2 cannot be turned off if it is already conducting. Note also that if positive voltages are applied to both the J and K inputs, neither Q1 nor Q2 can be triggered by a negative pulse applied at G. Because CR1 and CR2 can inhibit the clock pulses, they are often called *steering diodes*. This arrangement is called a clocked JK flip-flop.

BINARY RIGHT-SHIFT REGISTER

A binary right-shift register will shift any binary number to the right after it has been entered, and then do an "end-around" shift from the first flip-flop to the last flip-flop. The diagram for a 4-bit binary right-shift register is shown in Fig. 1-19. It operates in the same manner as explained previously for the left-shift register, except that an entered binary number proceeds to shift one place to the right with each clock pulse indefinitely. The binary number can be canceled when desired, as in the case of a left-shift register. It is instructive to observe some of the arithmetical properties of shift registers. Referring to Fig. 1-20, observe that when a binary number is shifted one position to the left, it becomes multiplied by 2. However, when the number is shifted

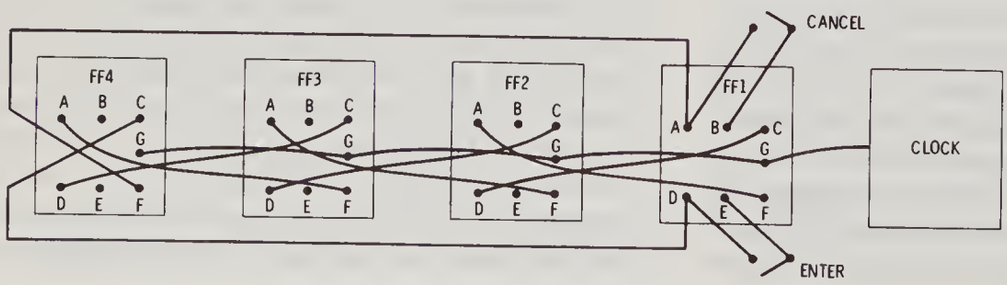


Fig. 1-19. Binary right-shift register arrangement.

one position to the right, it becomes divided by 2. Again, if the number is shifted two positions to the left, it becomes multiplied by 4, and so on.

It is evident that a shift register is a memory and will retain a binary number indefinitely. Additional circuitry can be employed to read out the memory on command. A shift register is also a delay device; it can be used to provide a delay for a chosen number of clock pulses with respect to a binary number that has been entered. Shift registers are always clocked. Entry of a binary number is often called "loading the shift register." Reading out the binary number is often called "unloading the shift register." The chief disadvantage of a shift register is that a delay is always involved between loading and unloading. In case the inherent delay is excessive for a particular computer application, another type of memory is employed; that is, other types of memories provide instant random access to any stored data.

TROUBLESHOOTING TECHNIQUES

1. No Output

A typical example of a *no-output* trouble symptom was noted previously; if the indicator lamp is burned out, the flip-flop displays a continuing "0" indication. The no-output trouble symptom can also be caused by a leaky or open capacitor. As an illustration, if C1 is open, Q1 cannot be triggered. An open capacitor can be found only on the basis of waveform checks with an oscilloscope. However, if the technician suspects that a capacitor is open, a useful quick check can be made by bridging (shunting) the suspected component with a known good capacitor. Then, if the flip-flop resumes normal operation, the suspicion is confirmed. Other less-probable causes of a no-output trouble symptom are the following:

a. Open or shorted steering diode, such as CR1 or CR2 in Fig. 1-4. Check by means of comparative resistance measurements.
b. Defective transistor, such as Q1, Q2, or Q3 in Fig. 1-4. Check by means of comparative dc voltage measurements.
c. Reversed supply-voltage polarity—transistors may be burned out in some circuits.
d. Subnormal supply voltage.
e. Resistor far off value; unlikely, but possible.
f. Break in printed-circuit conductor, or cold-solder connection.

2. Incorrect Output

The most common type of incorrect output is a "1" indication when a "0" should be indicated, and vice versa. Referring to Fig. 1-18, we see that this trouble symptom occurs if lamp I1 is on when it should be off, and vice versa. An incorrect output(s) is commonly caused by the following defects or malfunctions:

a. Marginal clock pulse amplitude; check with scope.
b. J and/or K pulse dropouts; check with scope.
c. Spurious negative pulses accompanying positive J or K pulses.
d. Intermittent steering diode, such as CR1 or CR2 in Fig. 1-18.
e. Marginal transistor; monitor the base waveforms with scope.

3. Occasional Incorrect Output

When there is an occasional incorrect output with extended periods of normal operation, the trouble is likely to be a mechanical intermittent due to a loose or cold-solder connection. Try tapping the malfunctioning circuit board and its associated circuit boards. If erratic response results, look for a poor connection, or replace the circuit board. However, if the fault cannot be localized to a specific board, replace the boards in the trouble area systematically until reliable operation is resumed. In this manner, the defective board can be found by elimination.

4. Intermittent Operation

Intermittent operation involves several kinds of come-and-go trouble symptoms. For example, a binary shift register, such as that depicted in Fig. 1-17, might operate erratically when it is started up and then settle down after a warm-up period. On the other hand, the shift register might operate normally for a while after it is started up and then gradually develop various trouble symptoms. After an interval of malfunction, the arrangement might again resume normal operation. Common causes for this general type of intermittent operation are the following:

a. Power-supply voltage fluctuation; monitor the supply voltage with a dc voltmeter.
b. Excessive ripple that increases or decreases at various times in the power-supply voltage; check ripple voltage and monitor with scope.

c. Thermally intermittent capacitor or transistor in clock generator; check clock waveform with scope.
d. High line resistance in elaborate arrangements with many flip-flops operating from the same power supply may be causing excessive common coupling. Check the ripple at the far end of the supply-voltage line. Cure: Use heavier connecting leads.

5. Stuck-At Readout

"Stuck at" is a frequently encountered trouble symptom. In other words, there is no response to trigger pulses. Referring to Fig. 1-18, we see that lamp I1 remains glowing in spite of normal clock, J, and K pulses in this trouble situation. Although there are numerous possible causes of "stuck-at" conditions, the most probable faults are:

a. Transistor Q3 shorted.
b. Transistor Q2 open.
c. Defective steering diodes.
d. Defective coupling capacitors.

6. Missing Numeral(s) in Readout

This trouble symptom is a form of "stuck-at" display in which the indicator lamp remains dark at all times instead of glowing continuously. With reference to Fig. 1-18, the most likely faults are:

a. Transistor Q3 open.
b. Transistor Q2 shorted.
c. Transistor Q1 open.
d. Lamp I1 burned out.

7. "Freewheeling" Operation

When a flip-flop operates as a free-running multivibrator, the trouble is caused by inadequate cutoff bias voltages. The steering diodes (Fig. 1-18) are prime suspects, plus spurious dc components in the J and K channels. Check the dc-voltage distribution in the affected flip-flop, and measure the front-to-back ratios of the steering diodes.

CHAPTER 2

Digital Logic Gates

A gate is a form of electronic switch that has two or more inputs and one output; the output depends upon the combination of pulses at the inputs. Although there are many possible gate configurations, the technician will encounter AND, OR, NAND, and NOR gates in the great majority of computer operations. These are the terms used in positive-logic systems. In positive logic, a "true" condition is defined as a binary number 1, and a "false" condition as a binary number 0. A binary number 1 corresponds to the most positive voltage condition, whereas a binary number 0 corresponds to the lowest voltage condition. On the other hand, in negative logic systems, the voltage states are the opposite of those noted above.

Common trouble symptoms caused by defects in digital logic arrangements are the following:

1. Nonfunctioning gate.
2. Incorrect response.
3. Intermittent operation.
4. Gate continuously on.

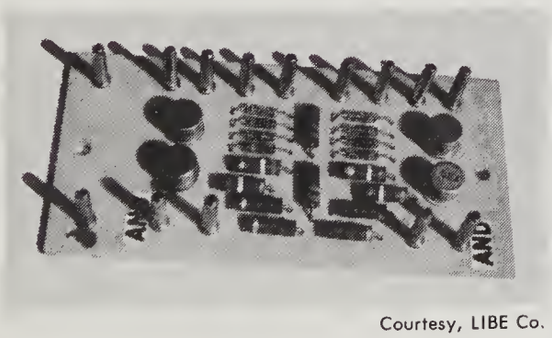


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Fig. 2-1. A pair of AND gates consisting of discrete components.

GENERAL DISCUSSION

Digital logic, or simply logic, is concerned with the circuitry and circuit actions used to perform computer operations such as addition, subtraction, multiplication, and division in binary arithmetic. These operations are also called symbolic logic. Gates are employed to control flip-flop states. Fig. 2-1 illustrates a pair of AND gates. A simple AND gate is diagrammed in Fig. 2-2. The gate consists of diodes CR1 and CR2, although the gate output is stepped up through transistors Q1 and Q2. These transistors also provide a NAND output in addition to the AND output. In other words, the NAND (NOT AND) output has opposite polarity (is 180° out of phase) from the AND output. In its resting state, the gate provides almost zero volts at its AND output terminal and almost +6 volts at its NAND output terminal. In its triggered state, the gate provides opposite output voltages—almost +6 volts at its AND output terminal and practically zero volts at its NAND output terminal.

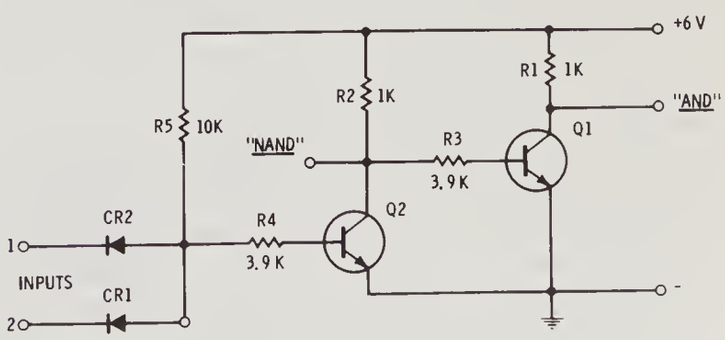


Fig. 2-2. Configuration of a typical AND gate.

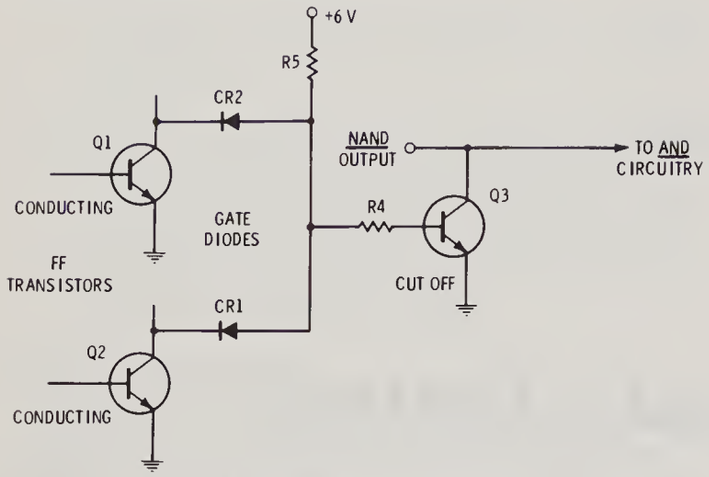
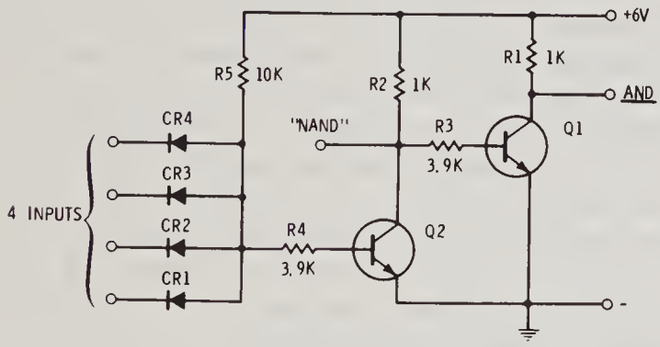


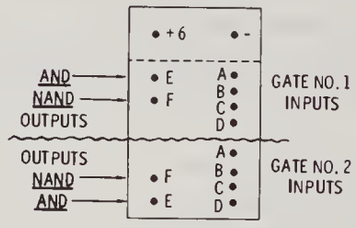
Fig. 2-3. Resting state of a simple AND gate.

To understand the response of the AND gate, refer to Fig. 2-3. In this example, the gate diodes CR1 and CR2 are being driven by a pair of flip-flops. Driving transistors Q1 and Q2 are conducting in the absence of input pulses. Accordingly, the collectors of Q1 and Q2 are practically at ground potential, which causes gate diodes CR1 and CR2 to conduct. Therefore, the base of Q3 is held nearly at ground potential, and Q3 is cut off. Now, for example, suppose that one input pulse occurs at the base of Q1 which suddenly becomes nonconducting. In turn, CR2 is cut off by the rise in positive voltage at the collector of Q1. Transistor Q3 remains cut off, nevertheless, because its base is effectively returned to ground via CR1 and Q2. However, suppose that input pulses to Q1 and Q2 occur at the same time; in other words, both Q1 and Q2 suddenly become nonconducting. Then, both CR1 and CR2 are cut off by the rise in collector potentials. Now, the base of Q3 becomes forward-biased via R4-R5, and Q3 goes into conduction. This makes the collector voltage of Q3 fall to zero, producing a NAND output. Also, the following AND output terminal rises to almost +6 volts, producing an AND output. To summarize briefly, an AND output will be produced only when CR1 *and* CR2 are nonconducting simultaneously.

Referring to Fig. 2-4, we observe that more than two input terminals can be provided for an AND gate. Four inputs are provided in this example. It follows from previous discussion that *all four* gate diodes must be nonconducting simultaneously in order to produce an AND output; that is, if any one of the input diodes is conducting, there will be no AND output. Of course, whenever an AND output is produced, a NAND output will also be produced with the output circuitry depicted in Fig. 2-4. Note that an AND output waveform is the same as the input waveform that actuates the AND gate. On the other hand, a NAND output is



(A) Configuartion.



(B) Circuit-board layout.

Fig. 2-4. An AND gate with four inputs.

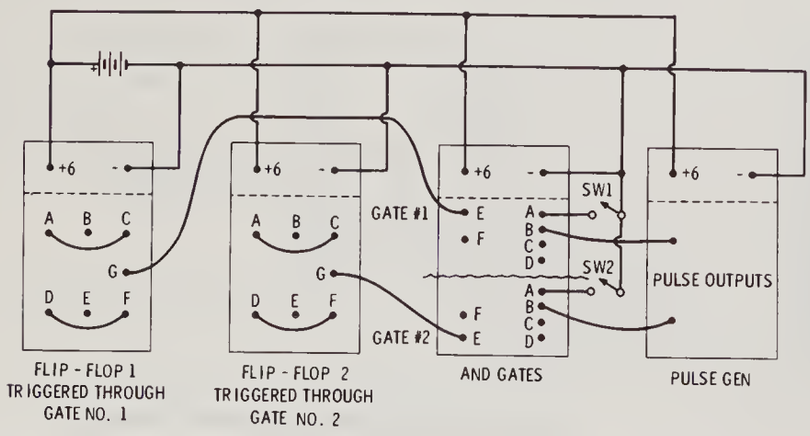
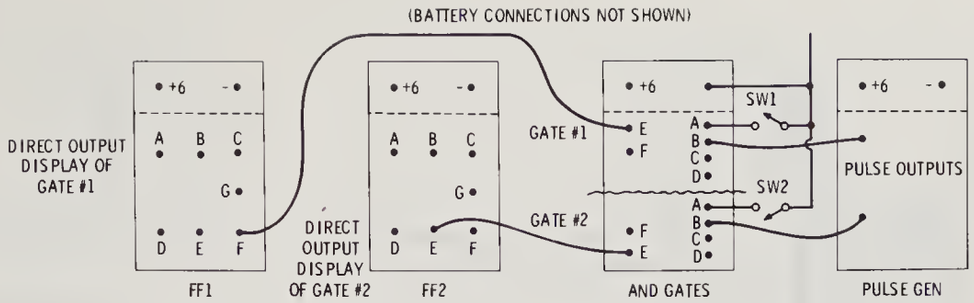


Fig. 2-5. Flip-flop triggered through AND gates.

(*A*) *Block diagram.*



(*B*) *Flip-flop Q1 transistor is driven.*

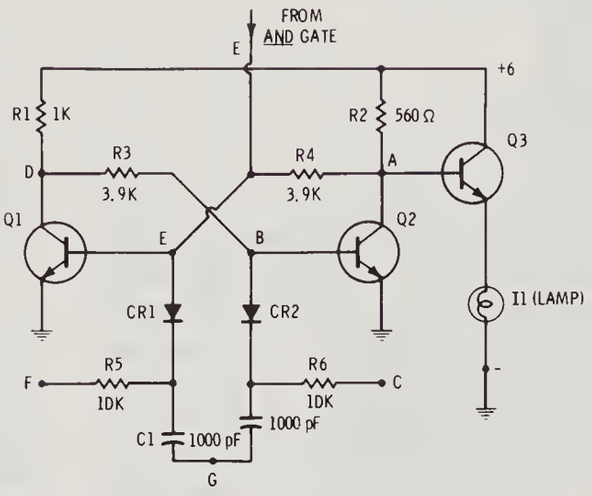


Fig. 2-6. Flip-flops triggered directly through AND gates.

of opposite polarity (180° out of phase) with the input waveform that actuates the AND gate. The circuit shown in Fig. 2-4A is the same as that used in each of the gates illustrated in Fig. 2-1. A corresponding terminal layout is shown in Fig. 2-4B.

It is instructive to observe the triggering of a pair of flip-flops by a pulse generator through a pair of AND gates, as shown in Fig. 2-5. When switches Sw1 and Sw2 are open, the flip-flop indicator lamps flash off and on alternately. In other words, the AND gates pass the outputs from the pulse generator. Since the pulse outputs are 180° out of phase, the flip-flops are triggered alternately. On the other hand, when switches Sw1 and Sw2 are closed, the AND gates block passage of the outputs from the pulse generator. In turn, the flip-flops are no longer triggered. Whether the flip-flops rest with their indicator lamps off or on depends on the state of each flip-flop at the instant that its corresponding gate switch is closed. Note that if Sw1 only is closed, flip-flop 1 ceases to change state but flip-flop 2 continues to be triggered. Of course, if Sw2 only is closed, flip-flop 2 ceases to change state but flip-flop 1 continues to be triggered.

Next, observe the direct-output flip-flop arrangement shown in Fig. 2-6. Note that the outputs from the AND gate do not trigger the flip-flops. Instead, the AND outputs drive the Q1 transistor in each flip-flop directly. Note that the outputs from the pulse generator are either high (approximately 6 volts) or low (approximately zero volts). Similarly, the outputs from the AND gates are either high or low. As shown in Fig. 2-6B, an AND-gate output is applied to the base of Q1 in the driven flip-flop. Terminals C and F are left unconnected in this arrangement. Transistor Q1 conducts when the AND-gate output is high, and cuts off when the AND-gate output is low. In turn, Q2 is driven by Q1; when Q1 conducts, Q2 cuts off, and when Q1 cuts off, Q2 conducts.

Referring to Fig. 2-6A, observe that when Sw1 is closed, gate No. 1 cannot drive FF1. In other words, the indicator lamp in FF1 remains dark, although the indicator lamp in FF2 flashes off and on. Next, if Sw2 is also closed, the indicator lamps in both FF1 and FF2 remain dark because gate No. 2 cannot drive FF2. Then, if both Sw1 and Sw2 are again opened, the indicator lamps in FF1 and FF2 resume flashing on and off alternately. Note that although the same general cir-

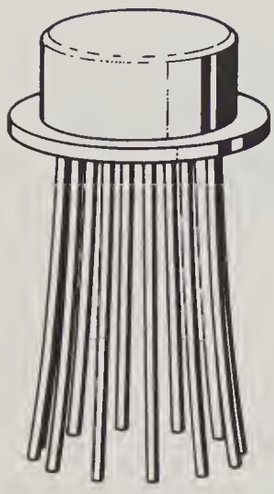
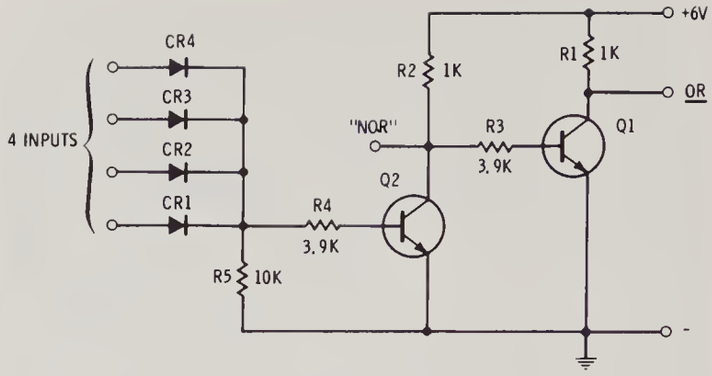


Fig. 2-7. Gates and flip-flops are fabricated in IC form.

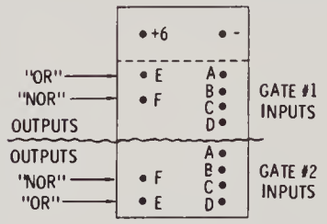
cuit actions are provided by the triggered arrangement depicted in Fig. 2-5, there is one important difference. When Sw1 is closed in this triggered configuration, the indicator lamp in FF1 might then glow continuously or it might be dark continuously. This condition depends solely on the state of the flip-flop at the instant that Sw1 is closed. Similarly, when Sw2 is closed in the triggered configuration, the indicator lamp in FF2 might glow continuously or it might be dark continuously. Thus, if the lamp happens to be glowing at the instant that the switch is closed, it will continue to glow, or vice versa. Note in passing that AND gates such as those pictured in Fig. 2-1 are also available in integrated-circuit form. An AND gate in IC form is shown in Fig. 2-7. Flip-flops are also available in IC form, as explained in greater detail subsequently.

OR GATE

Another basic digital arrangement is the OR gate, as exemplified in Fig. 2-8. Observe that its circuitry is somewhat similar to that of the AND gate shown in Fig. 2-4. However, the OR configuration has an important difference in that the diodes are oppositely polarized; note also that the diodes are returned to ground, instead of to the supply voltage. In turn, the OR gate has a different response to high and low logic levels as compared with the AND gate. In other words, the OR gate in Fig. 2-8 will produce a positive output pulse if any one or all of the inputs are driven positive. By way of comparison, the AND gate depicted in Fig. 2-4 produces a positive output pulse only if all of the inputs are driven positive.



(A) Configuration.

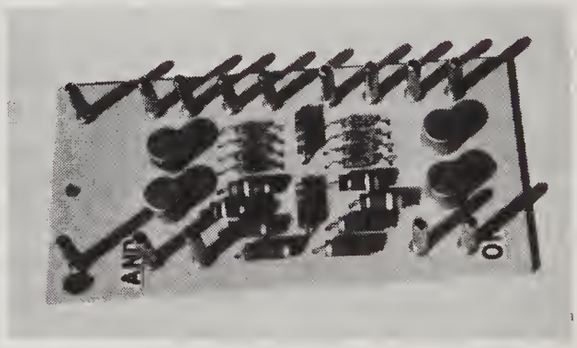


(B) Circuit-board layout.

Fig. 2-8. An OR gate with four inputs.

As a practical note, all four of the inputs do not have to be wired into a digital circuit (Figs. 2-4 and 2-8). For example, three of the inputs might be utilized, or only two of the inputs. Unused inputs are merely left open or "floating." As an illustration, only two of the inputs for each of the AND gates in Fig. 2-6 are wired into the digital circuit.

Observe that the OR gate configuration shown in Fig. 2-8 has a NOR output as well as an OR output.



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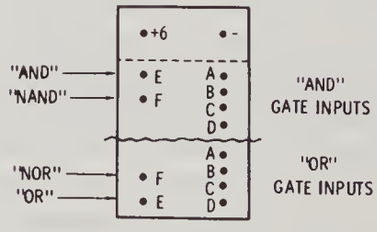
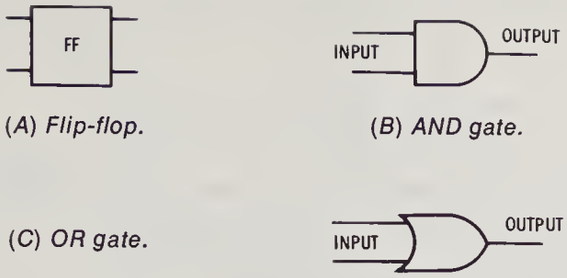
(A) Photograph.



(B) Terminal identification.

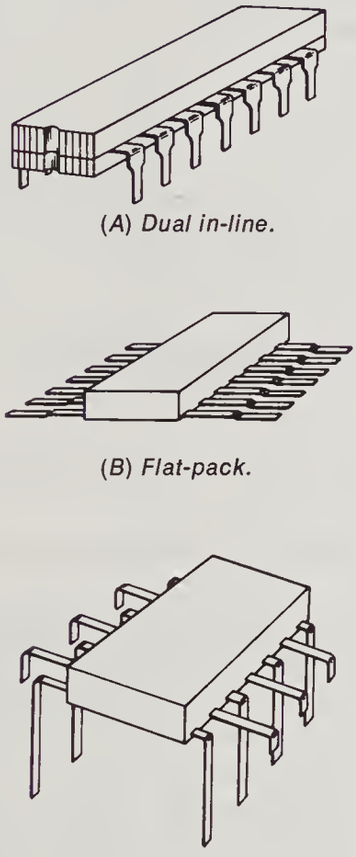
Fig. 2-9. AND & OR gate circuit board.



(A) Flip-flop. (B) AND gate.

(C) OR gate.

Fig. 2-10. Simplified digital-logic symbols.



(A) Dual in-line.

(B) Flat-pack.

(C)Staggered-lead.

Fig. 2-11. Flip-flops and gates are fabricated in various types of IC packages.

The NOR (NOT OR) output is oppositely polarized, or it is 180° out of phase with the OR output. It is instructive to observe the comparative responses of an AND gate and an OR gate in a basic digital configuration. For this purpose, an arrangement will be analyzed that utilizes the AND & OR circuit board illustrated in Fig. 2-9.

Consider the responses that will be obtained when the AND gates in Fig. 2-6 are replaced by the AND & OR circuit board shown in Fig. 2-9. In this situation, FF1 is driven through an AND gate but FF2 is driven through an OR gate. As would

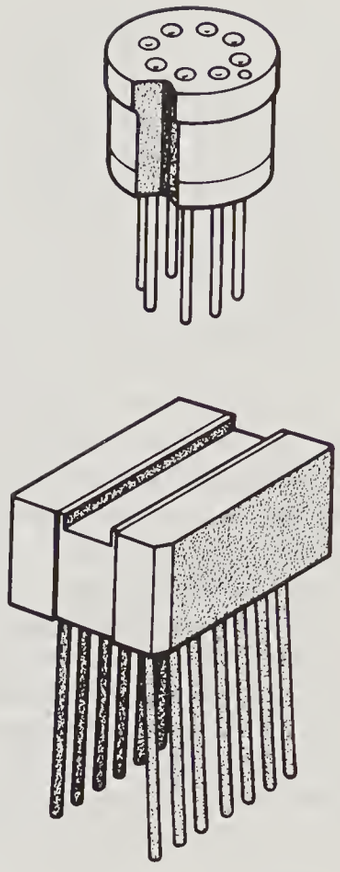
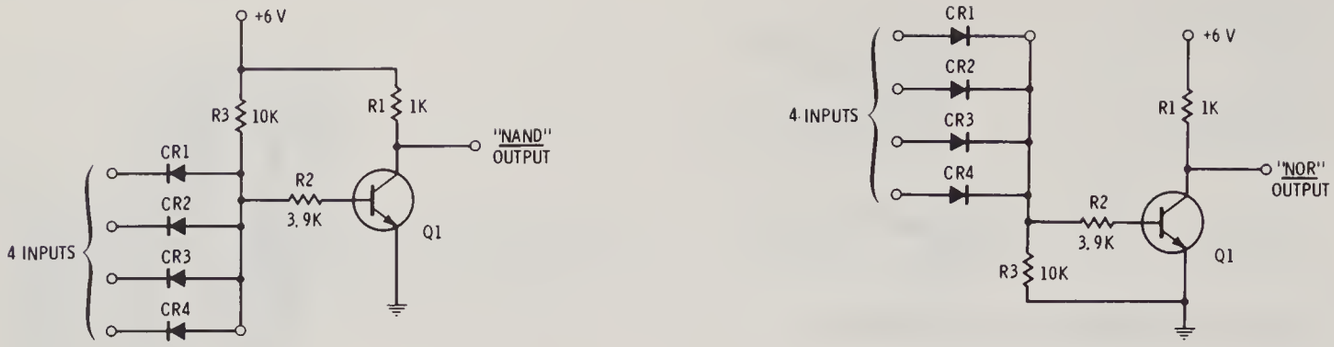


Fig. 2-12. Typical IC sockets.

be expected, the flip-flop indicator lamps flash on and off alternately as long as Sw1 and Sw2 are open. When Sw1 and Sw2 are closed, only the FF2 indicator lamp flashes on and off. As noted previously, closure of Sw1 causes passage of the driving pulse through the AND gate to be blocked. However, closure of Sw2 has no effect on the operation of the OR gate. This is the basic difference between AND-gate and OR-gate response. Note that flip-flops, AND gates, and OR gates are commonly represented by the simplified symbols shown in Fig. 2-10. Although two-input gates are depicted, any number of inputs might be shown for particular applications. Flip-flops and gates are also available in flat-pack IC form, as shown in Fig. 2-11.

Trouble in digital IC circuits may involve poor mechanical contacts, in addition to device failure. In other words ICs may be soldered into the circuit board, or they may be plugged into sockets as shown in Fig. 2-12. From the standpoint of reliability, it is preferable to solder ICs into the circuit board. On the other hand, digital ICs are



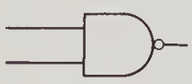
(A) NAND circuit. *(B) NOR Circuit.*

Fig. 2-13. Typical NAND and NOR gates.

subject to the possibility of device failure. This is particularly true of ICs connected to input and output terminals of the equipment. Therefore, troubleshooting is considerably facilitated by mounting ICs in sockets. However, reliability is impaired by socket mounting because shock or vibration can cause ICs to pop completely out of their sockets. Also, mechanical contacts can become defective, although an IC remains fully inserted into its socket. The technician should keep these points in mind when evaluating trouble symptoms in a unit that employs socket-mounted ICs.

NAND & NOR GATES

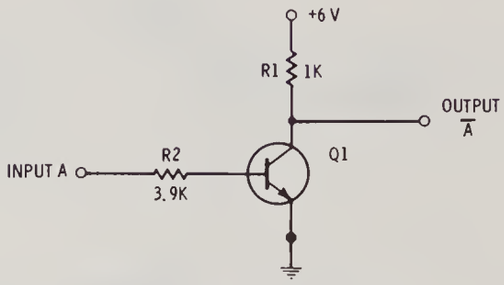
Typical circuits for NAND (NOT AND) and NOR (NOT OR) gates are shown in Fig. 2-13. As noted previously, a NAND gate functions in the same manner as an AND gate, except that it provides an inverted output. Similarly, a NOR gate functions in the same manner as an OR gate, except that it provides an inverted output. Thus, if positive-going pulses are applied to each input of the NAND gate (Fig. 2-13), the gate responds by developing a negative-going pulse at the collector of Q1. If a positive-going pulse is applied to the NOR gate, the gate responds by developing a negative-going pulse at the collector of Q1. Note that the NAND and NOR gates shown in Fig. 2-13 are the same as the Q2 circuitry depicted in Figs. 2-4 and 2-8. The NAND and NOR gates are commonly represented by the simplified symbols shown in Fig. 2-14. In other words, the small circle at the output terminal means NOT.



(A) NAND gate.

(B) NOR gate.

Fig. 2-14. Simplified digital-logic symbols.



(A) Basic configuration.

(B) Simplified symbol.

Fig. 2-15. Circuit for an inverter gate.

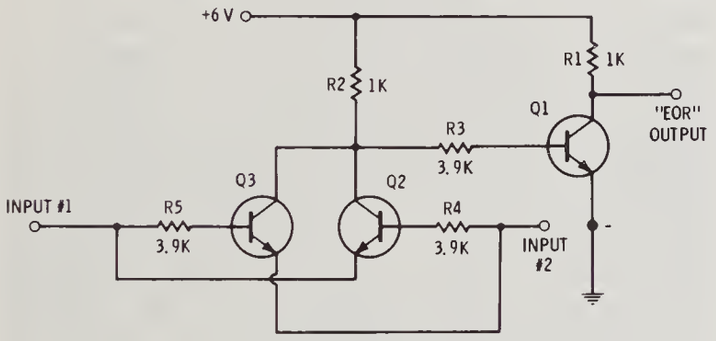
Next, observe the inverter gate circuit shown in Fig. 2-15. Only one input is utilized for this type of gate. The purpose of an inverter gate is to change an AND input into a NAND output or to change an OR input into a NOR. With the diodes omitted and the input signal applied directly to the base of the transistor, an inverter gate has the same circuitry as Q2 in Figs. 2-4 and 2-8. Note in Fig. 2-15 that an input-pulse A is indicated; in turn, an output-pulse $\bar{A}$ is indicated. The symbol $\bar{A}$ means NOT A. For example, A might correspond to a change from a zero-volt level to a +6-volt level. In turn, $\bar{A}$ would correspond to a change from a +6-volt level to a zero-volt level. This is just another way of saying

that a binary 1 input to the inverter results in a binary 0 output.

EXCLUSIVE OR GATE

An EXCLUSIVE OR (EOR) gate differs from an OR gate in that its output will be a binary 1 if and only if *one* of its inputs is a 1. In other words, suppose that an EOR gate has two inputs. A binary 1 output will be obtained if either of these inputs is a 1 and the other is a 0. On the other hand, a binary 0 output will be obtained if both of these inputs are a binary 1. An EOR gate might have three, four, or more inputs, and its response can be summarized as follows: *If one and only one of the inputs to an* EOR *gate is a 1, then the output is a 1. However, if more than one input is a 1, or if all of the inputs are 0, then the output is 0.*

A simple circuit for an EOR gate with two inputs is shown in Fig. 2-16. In its resting state, transistors Q2 and Q3 are cut off and Q1 is conducting. In turn, the EOR output is at ground potential, or 0. Next, suppose that a 1 input (+6 volts) is applied to input No. 1. The emitter of Q3 is effectively grounded through the 0 source at input No. 2. Accordingly, Q3 conducts and the base of Q1 falls to ground potential. Transistor Q1 cuts off, and the EOR output rises to +6 volts. However, if an input (+6 volts) is applied to both input No. 1 and input No. 2, the emitters and bases of both Q2 and Q3 are placed at +6-volts potential. Since the base and emitter of each transistor are at the same potential, both transistors are cut off, and Q1 continues to conduct. This is just another way of saying that if both inputs are 1, the EOR output is a 0.



(*A*) *Basic circuit.*

(*B*) *Simplified symbol.*

Fig. 2-16. An EOR gate configuration.

An oscilloscope check will show that spurious spikes (false pulses) are produced by the circuit in Fig. 2-16 when an input signal is applied. Therefore, this particular circuit is suitable only for operating an indicator lamp. If it is used to trigger another unit of digital equipment, the false pulses that are generated by this EOR gate will cause incorrect operation. For this reason, the more elaborate EOR gate depicted in Fig. 2-17 is generally more useful. This configuration is called a *summation* gate, *sum* gate, *parity* gate, or *half adder*. Since this circuit does not produce spurious spikes, it can be used to trigger other units of digital equipment. Note that a *sum* gate with two inputs has the same response as the aforementioned EOR gate.

The configuration in Fig. 2-17 is called a *sum* gate because it is used in binary adder arrangements, as explained in greater detail subsequently. *Parity* means a distinction between even and odd numbers of binary 1's or 0's. In this example, only two inputs are provided but the principle of parity is exemplified by the following responses: In case

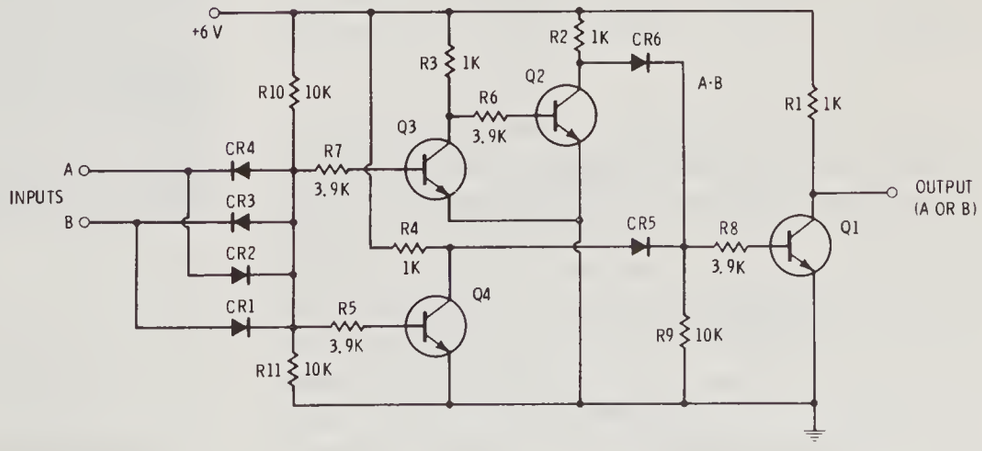


Fig. 2-17. Configuration for a sum gate.

one of the inputs is a binary 1, the number of inputs is odd and the output is a binary 1. On the other hand, if both of the inputs are binary 1's, the number of inputs is even and the output is a binary 0. When a *parity* gate has several inputs, its response can be summarized as follows: *If all binary 1 inputs have odd parity, then the output is a binary 1, if all binary inputs have even parity, then the output is a binary 0.* Applications for parity checks are explained subsequently.

Next, consider how the sum gate in Fig. 2-17 functions. In its resting state, with the A and B inputs at ground potential (binary 0's), transistors Q3 and Q4 are cut off. In turn, Q2 conducts because Q3 is cut off and Q1 conducts because Q4 is cut off. Accordingly, the output from Q1 is a binary 0. Next, suppose that a binary 1 is applied only to input A. In turn, Q4 conducts via CR2 and Q1 cuts off because both Q2 and Q4 are conducting. Consequently, the output from Q1 is a binary 1. Now, suppose that a binary 1 is applied only to input B. The result is that Q4 conducts via CR1, so that Q1 cuts off and its output is a binary 1. However, in case that binary 1 inputs are applied to both A and B, CR3 and CR4 no longer conduct and Q3 is thrown into conduction. Accordingly, Q2 becomes cut off and Q1 continues to conduct via CR6. Therefore, the output from Q1 is a binary 0.

It is instructive to observe why the sum gate in Fig. 2-17 is called a *half adder*. As noted previously, the binary addition of 1 and 0 is equal to 1; the binary addition of 0 and 1 is equal to 1; and the binary addition of 1 and 1 is equal to 0 with 1 to carry. These basic facts of binary arithmetic are evident from the following notation:

Decimal	Binary
0	0
1	1
2	10

In other words, the binary number 10 which corresponds to the decimal number 2 consists of the sum of a pair of binary 1's, and this sum is written as a binary 0 with a binary 1 carried to the next higher position. Now, observe in Fig. 2-17 that the sum gate can add a binary 1 to a binary 0, or can add a binary 0 to a binary 1, but cannot completely add a binary 1 to a binary 1. In other words, the sum gate produces the binary 0 portion of the answer, but does not supply the binary carry 1. For this reason, the sum gate is called a half adder, meaning that it must be elaborated before it can function as a complete (full) adder.

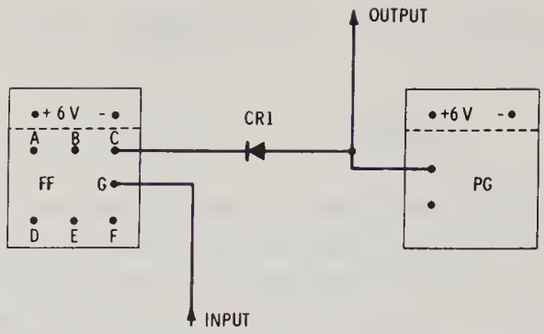


Fig. 2-18. A halt-command arrangement.

BASIC SENSE AND COMMAND CIRCUITRY

A *command* is a signal or a series of signals resulting from an instruction. An *instruction* is a suitable signal that causes certain digital operations to be performed. As an illustration, a command may cause a flip-flop to change state, or may cause a binary addition or a binary subtraction to be performed, or may cause a "halt" in a sequential operation. A *sense* is a signal or a series of signals that controls the execution of a command. For example, a sense configuration can determine whether or not a register contains a binary number. Thus, it typically determines the state of the flip-flops. Observe the halt command arrangement shown in Fig. 2-18. The flip-flop has the configuration depicted in Fig. 2-6. Thus, CR1 is connected to the collector of transistor Q2 in the flip-flop. When the flip-flop is on, the collector potential of Q2 is approximately 6 volts and diode CR1 is reverse-biased. On the other hand, when the flip-flop is off, the collector is essentially at ground potential, causing CR1 to be forward-biased. Therefore, there is a pulse output from the pulse generator when the flip-flop is on, but there is no pulse output when the flip-flop is off because CR1 holds the output at ground po-

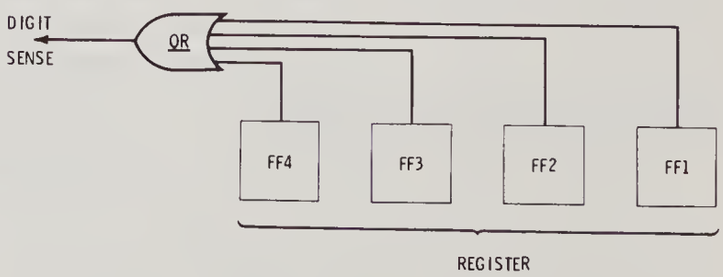


Fig. 2-19. Another example of a sense configuration.

tential. Note that the CR1 circuit functions as a sense arrangement; it supplies a *halt* command when the flip-flop is off.

Another example of a sense configuration is shown in Fig. 2-19. This is called a *digit sense*, and its function is to determine if there is a binary number in the register. The sense configuration is simply an OR gate with its inputs driven by the "true" outputs of the flip-flops in the register. Note that the true output is from terminal A (collector of Q2) in Fig. 2-6. Thus, there is a high-level (1) input to the OR gate in Fig. 2-19 whenever there is one or more glowing indicator lamps in the register. In turn, there will be a high-level output from the OR gate. However, if all the indicator lamps in the register are dark, all the inputs to the OR gate will be at low level and the OR gate output will also be at low level. Typical applications of sense and command circuitry are encountered in adders and decimal counters, as explained in the next chapter.

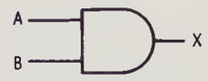
NEGATIVE LOGIC

Practical digital troubleshooting procedures are occasionally concerned with negative logic, instead of positive logic, or with a combination of positive logic and negative logic. There are two conventions defining logic levels. According to *positive-logic* convention, a more-negative potential is called logic-low, and a more-positive potential is called logic-high. For example, +5 volts might be called logic-high, and zero volts might be called logic-low. Most digital equipment employs positive logic, in which a less-positive potential is called logic-low, and a more-positive potential is called logic-high. According to the other convention, *negative logic*, a logic-high level is defined as the more-negative potential, and the logic-low level is the more-positive potential.

Consider next the distinction between positive logic and negative logic. In the following example, truth tables will be compared; these truth tables will be compiled on the basis of +5-volt and ground potentials. A truth table for a 2-input positive-logic AND gate (Fig. 2-20) is written:

A	*B*	*X*
Gnd	Gnd	Gnd
Gnd	+5 V	Gnd
+5 V	Gnd	Gnd
+5 V	+5 V	+5 V

(*A*) *Positive-logic levels.*



(*B*) *Logic symbol.*

Fig. 2-20. A 2-input positive-logic AND gate.

When positive logic is used, the more-positive voltage is called "1," and the less-positive voltage is called "0." Thus, in the truth table for the positive-logic, ground corresponds to 0, and +5 V corresponds to 1. Therefore, this truth table may be written in the form:

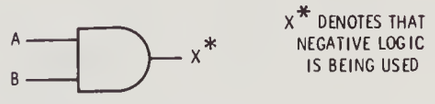
A	*B*	*X*
0	0	0
0	1	0
1	0	0
1	1	1

However, in case negative logic is used, the definitions and notations are different. It is helpful to consider next how a 2-input AND gate operates when negative logic is utilized. In negative logic, the more-positive voltage is called logic-low, or 0. The less-positive voltage is called logic-high, or 1. Thus, to continue our example, the logic-high state will be ground, and the logic-low state will be +5 V. In turn, the truth table for our 2-input AND gate (Fig. 2-21) is written for negative-logic operation as follows:

A	*B*	*X*
Gnd	Gnd	Gnd
Gnd	+5 V	Gnd
+5 V	Gnd	Gnd
+5 V	+5 V	+5 V

Thus far, it might seem that there is really no difference between positive logic and negative

(*A*) *Negative-logic levels.*



(*B*) *Logic symbol.*

Fig. 2-21. A 2-input negative-logic AND gate.

(A) Positive-logic levels.

(B) Logic symbol.

Fig. 2-22. A 2-input positive-logic OR gate.

logic. However, here is where the basic distinction occurs. In negative logic, ground corresponds to 1, and +5 V corresponds to 0. In turn, the truth table for a 2-input AND gate in negative logic is written:

A	*B*	*X**
1	1	1
1	0	1
0	1	1
0	0	0

where X* denotes that negative logic is utilized.

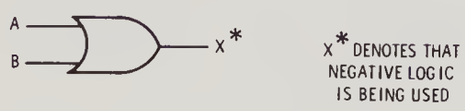
Note that the truth table for a negative-logic AND gate is "opposite" from the truth table for a positive-logic AND gate, in that the 1's become 0's, and the 0's become 1's. Referring to Fig. 2-22, consider the truth table for a 2-input positive-logic OR gate:

A	*B*	*X*
1	1	1
1	0	1
0	1	1
0	0	0

Observe carefully that this truth table for a 2-input positive-logic OR gate is the same as the truth table that was shown for a 2-input negative logic AND gate.

Next, referring to Fig. 2-23, consider the truth table for a 2-input negative-logic OR gate:

(A) Negative-logic levels.



(B) Logic symbol.

Fig. 2-23. A 2-input negative-logic OR gate.

A	*B*	*X**
0	0	0
0	1	0
1	0	0
1	1	1

Where X* denotes that negative logic is utilized.

Observe carefully that this truth table for a 2-input negative-logic OR gate is the same as the truth table that was shown for a 2-input positive-logic AND gate.

Therefore, we have established the following basic digital-logic laws:

The truth table for a negative-logic AND *gate is the same as the truth table for a positive-logic* OR *gate.*

The truth table for a negative-logic OR *gate is the same as the truth table for a positive-logic* AND *gate.*

This type of demonstration is easily extended to establish the additional basic digital-logic laws:

The truth table for a negative-logic NAND *gate is the same as the truth table for a positive-logic* NOR *gate.*

The truth table for a negative-logic NOR *gate is the same as the truth table for a positive-logic* NAND *gate.*

It is very important for the digital troubleshooter to recognize that, in any case, the gates remain the same and that no new electrical laws are involved. It is only a matter of definition whether ground, for example, shall represent 0 or 1, and whether +5 V, for example, shall represent 1 or 0. The definition that is chosen in a particular application *does* change the input/output relationships of a gate. This change in relationship is such that an AND gate in positive logic will be regarded as an OR gate in negative logic. This is obviously a vital point for the troubleshooter, who tests the response of a gate by pulsing its inputs to determine whether its output is correct or incorrect.

To repeat an important point, the troubleshooter should not confuse positive and negative operating levels with positive logic and negative logic. In other words, a positive logic *level,* such as the range from ground to +5 V, might employ either *positive logic* or *negative logic.* Again, a negative logic *level,* such as the range from ground

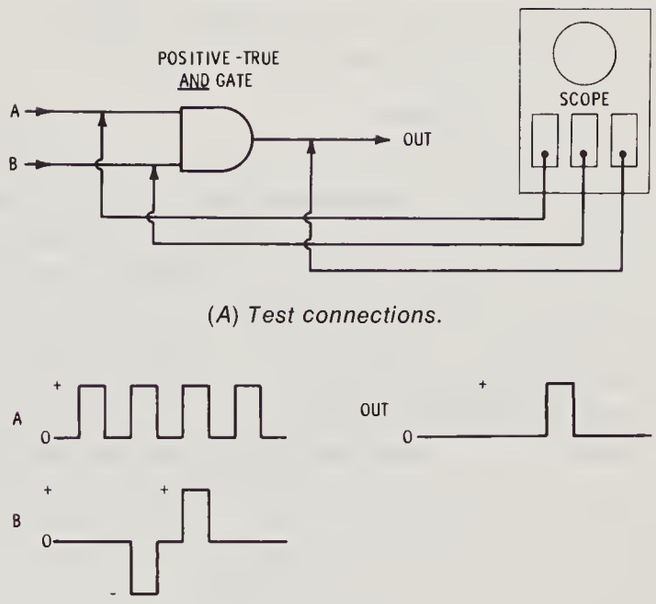
to −5 V, might employ either *positive logic* or *negative logic*. As another illustration, a positive logic *level* from +0.2 V to +2 V might employ either *positive logic* or *negative logic*. Or, a negative logic level from −0.2 V to −2 V might employ either *positive logic* or *negative logic*.

TROUBLESHOOTING TECHNIQUES

1. Nonfunctioning Gate

A nonfunctioning gate produces no output pulses in response to applied input pulses. It is important to avoid confusing a nonfunctioning gate with no output due to "bad-level" input pulses. In other words, input pulses that have subnormal amplitude will fail to operate the gate. It is essential to know the digital equipment being serviced or to refer to the servicing data in this regard. Typically, supply voltages may be 12 volts, whereas the pulse amplitudes (logic voltages) may be 5 volts or less. For a particular digital system, a binary 0 might correspond to a zero-volt level, and a binary 1 might correspond to a 3-volt level. In this example, an input of 3 volts or more to an OR gate represents "good-level" pulses, whereas an input of 2 volts would represent "bad-level" pulses. Input and output pulses can be checked with a calibrated oscilloscope. Note that pulses may be wide or narrow, depending upon the particular digital equipment. The oscilloscope must have sufficient bandwidth to display the pulses without attenuation or substantial distortion.

It is evident that a gate must be identified before its response can be evaluated. For example, the response of the AND gate depicted in Fig. 2-4 is not the same as that of the OR gate shown in Fig. 2-8. Again, the sum gate shown in Fig. 2-17 has still another pattern of response. Suppose that a gate falls under suspicion and that it is identified as an AND gate. In such a case, we recognize that all of the inputs must be pulsed simultaneously in order to obtain an output pulse. We assume here that we are utilizing responses to pulse trains produced by the digital equipment itself (no external pulses are being injected into the circuits). Therefore, it is necessary in this situation to operate or program the equipment in such a manner that the necessary input pulses are applied to the gate under test. Accordingly, a multiple-trace oscilloscope is helpful (although not absolutely essential) to observe both the input and output pulses simultaneously. Fig. 2-24 shows



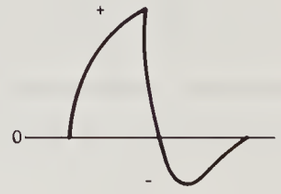
(*A*) *Test connections.*

(*B*) *Example of normal test display.*

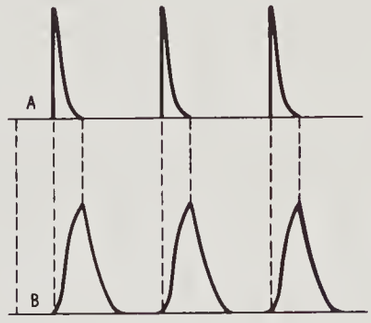
Fig. 2-24. Checking AND gate response with a multiple-trace scope.

a typical checkout of an AND gate with a normal output. Note that if output pulses are absent under the test condition, the gate is evidently nonfunctioning. Common causes for a nonfunctioning gate are:

a. IC not fully inserted into its socket.
b. Cold-soldered connection.
c. Broken printed-circuit conductor.
d. Leakage or short circuit between printed-circuit conductors.



(*A*) *A seriously distorted pulse.*



(*B*) *Pulse peaks mistimed.*

Fig. 2-25. Distorted and mistimed pulses.

e. Open or shorted semiconductor device.
f. Short-circuited load at gate output.

2. Incorrect Response

When a gate functions but produces incorrect response, there are two basic types of faults to be considered. For example, the input pulses that are applied to the gate might be seriously distorted, or the pulses might be mistimed, or they might have subnormal amplitudes as noted previously. On the other hand, the input pulses may be within normal tolerances, in which case the trouble will be found in the gate (provided that the supply voltage to the gate is normal). Therefore, it is good practice to check the supply voltage first and then observe the input pulses that are being applied to the gate. Fig. 2-25 shows seriously distorted and mistimed pulses. Since this topic is concerned with gate defects, troubleshooting distorted pulse trains will be discussed later. Common causes for incorrect gate responses are:

a. Digital module not fully inserted into socket.
b. Corroded module contacts.
c. Mechanically strained or damaged socket.
d. Defective discrete-components module; diode(s) with poor front-to-back ratio, such as CR1 through CR4 in Fig. 2-8.
e. Defective transistor, such as Q1 or Q2 in Fig. 2-8.
f. Off-value resistor, such as R6 in Fig. 2-17 (not likely, but possible).

3. Intermittent Operation

Intermittents may be mechanical or thermal in nature. A mechanical intermittent results from an uncertain contact; the gate response may become normal or abnormal when the circuit board, IC, or various discrete components are tapped. A thermal intermittent does not change as a result of vibration or shock. Instead, it responds to heat and cold. For example, a gate might operate normally for several minutes after the digital equipment is first turned on. Then, after a warm-up period, the gate might develop an incorrect output or no output. In such a case, spraying the gate package or components with a circuit coolant will often restore normal operation for a while. Mechanical intermittents are sometimes caused simply by dirty or corroded module contacts. Therefore, it is better to track down the cause of the intermittent than to just replace the module without knowing what was causing the trouble symptom.

4. Gate Continuously On

This trouble symptom is a form of nonfunctioning gate condition. Although normal input pulse trains are applied to the gate, its output remains continuously at high level regardless of the input level. Common causes of this malfunction are:

a. Open transistor, such as Q1 in Fig. 2-4.
b. Shorted transistor such as Q2 in Fig. 2-4.
c. Broken printed-circuit conductor, such as the emitter-ground lead in Fig. 2-8.
d. Shorted printed-circuit conductors, such as the base and emitter conductors of Q1 in Fig. 2-8.
e. Open (or excessively high-value) resistor, such as R8 in Fig. 2-17.
f. Incorrect type of replacement gate (IC module) plugged into socket.

CHAPTER 3

Binary Adders, Subtracters, and BCD Counters

As noted in Chapter 1, an up counter serves as a simple binary adder. More-elaborate digital adders include various gate arrangements. Other types of adders are called binary adders, full adders, serial adders, and parallel adders. Binary subtraction involves a modified form of addition, as will be discussed later. A binary-coded decimal counter (bcd counter) expresses each decimal digit of a number by binary numbers in which each decimal digit is represented by four binary bits. It includes logic gates and uses a counter arrangement to operate decimal-system digital displays. A binary adder, which is the simplest form of adder, has two inputs. A full adder has three inputs and accepts a "carry" as well as the two numbers to be added. Serial binary addition utilizes the bits (binary digits) which represent each number to be added. These bits are in the form of pulses in a train. Parallel binary addition is comparatively rapid because it is not accomplished on the basis of sequential pulses in trains. Instead, binary numbers are stored in registers, and logic gates are utilized to obtain the sum in a simultaneous operation.

Common trouble symptoms caused by defects in binary adders, subtracters, and bcd counters are:

1. Incorrect readout.
2. No readout.
3. Erratic operation.
4. Malfunction on large numbers only.

NONGATED BINARY ADDER

A simple digital adder arrangement, called a nongated binary adder, is shown in Fig. 3-1. It includes a binary-up counter, a binary-down counter, a halt command flip-flop, and a pulse generator. To program the adder, a binary number is entered into the *addend register* (up counter). The addend register is then cleared, as will be explained subsequently. Then, another binary number is entered into the addend register. Again, the addend register is cleared, and the sum of the two binary numbers appears automatically in the *accumulator*. If desired, a third binary number can be entered into the addend register. When the addend register is again cleared, the total sum appears in the accumulator. Of course, the accumulator has a limited capacity, and will eventually "overflow." After the desired sum has been obtained, the accumulator is cleared, as will be explained, and the adder is ready for a new program.

The operation of the nongated binary adder will now be discussed in detail. When Sw1 is closed, no halt command can occur, and the addend register counts clock pulses from 1 to 15 and then resets (clears) and starts over again. This process will continue as long as Sw1 is closed. On the other hand, if Sw1 is opened, the addend register will count up to 15, clear, and then stop. In other words, when Sw1 is opened, the halt flip-flop will stop the clock as soon as it receives a trigger pulse from flip-flop B4. Next, consider the response of the accumulator. When Sw1 is closed, no halt command can occur, and the accumulator counts clock pulses from 15 down to 0 and then starts over again. However, when Sw1 is opened, the accumulator will continue to count clock pulses only until the addend register is clear. As soon as

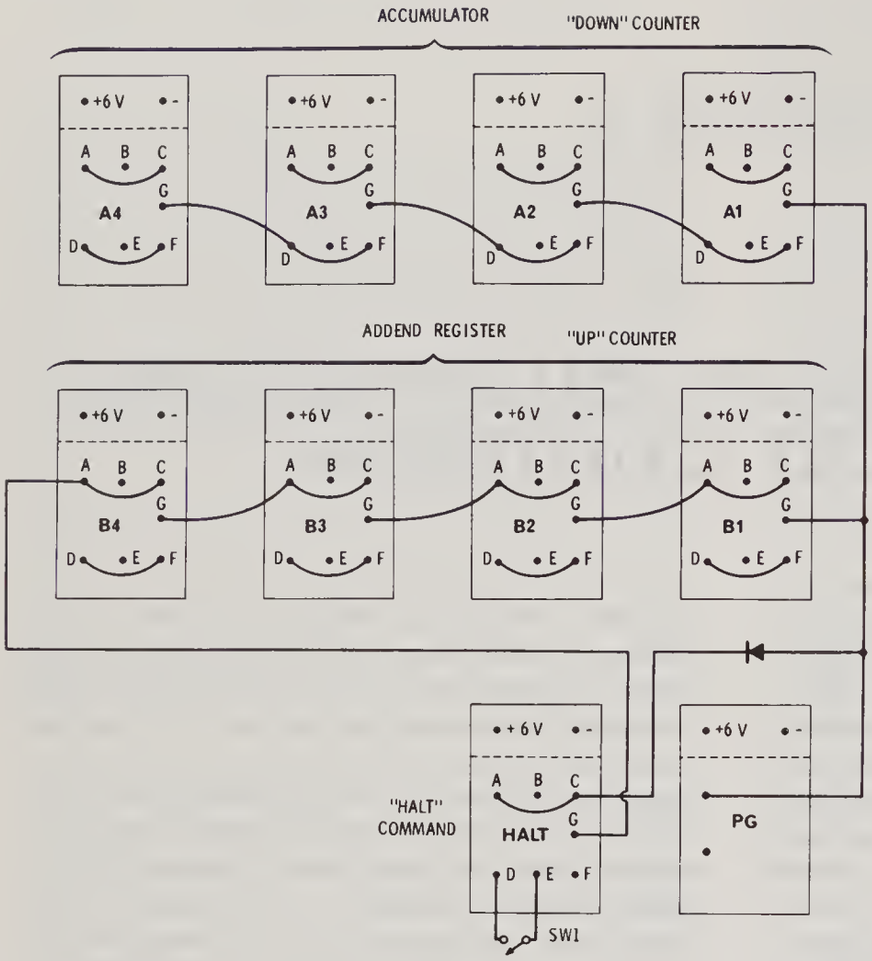
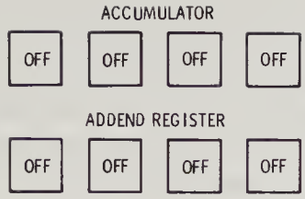


Fig. 3-1. Arrangement of a nongated binary adder.

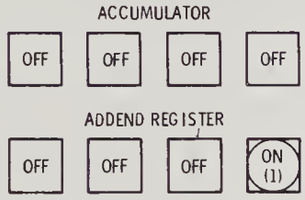
the addend register clears, the accumulator stops counting because the halt command stops the clock.

Consider how binary numbers that have been entered into the addend register are transferred into the accumulator. Referring to Fig. 3-2, we start with the addend register and the accumulator cleared. In other words, all of the indicator lamps are dark. Then, we may enter a number such as a binary 1 into the addend register, as shown in Fig. 3-2B. This is done by momentarily connecting terminals D and E together in flip-flop B1 (Fig. 3-1). Next, this binary number 1 is transferred into the accumulator by momentarily closing Sw1 on the halt fiip-flop. Note that when Sw1 is closed, clock pulses start. Although Sw1 is opened promptly, the clock pulses will continue, and both the addend register and the accumulator are triggered until the addend register overflows. At this time, the halt flip-flop is triggered by flip-flop B4 (Fig. 3-1), and the halt flip-flop stops the clock. During the time that the addend register is being cleared, the accumulator is counting down from 15 to 1. The clock pulse that finally clears the addend register leaves the flip-flop A1 lamp glowing (Fig. 3-1). Thus, the accumulator indicates the binary number 1 after the clock stops.

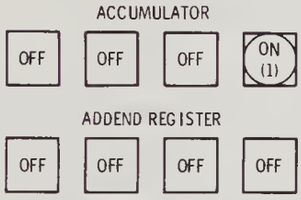
Now, consider how the binary number 2 may be added to the binary number 1 that is stored in the accumulator. Referring to Fig. 3-3, we start by entering the binary number 2 in the addend register. This is done by momentarily connecting terminals D and E together on flip-flop B2 (Fig. 3-1). Next, this binary number 2 is transferred into the accumulator by momentarily closing Sw1 of the halt flip-flop (Fig. 3-1). When Sw1 is closed, clock pulses start. Although Sw1 is opened promptly, the clock pulses will continue to trigger both the addend register and the accumulator until the addend register overflows. Thereupon, the halt flip-flop is triggered by flip-flop B4 (Fig. 3-1), and the halt flip-flop stops the clock. During the time that the addend register is being cleared, the accumulator is counting down from 1, through "clear," and down to 3. Accordingly, the accumulator then indicates the sum of 2 and 1, or 3. As a result, the lamps in flip-flops A2 and A1 (Fig. 3-1) remain glowing. If desired, still another



(A) Addend register cleared; accumulator cleared.

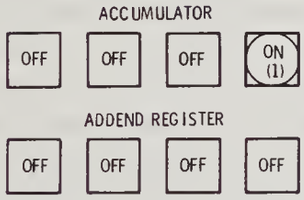


(B) Binary number 1 entered into addend register.

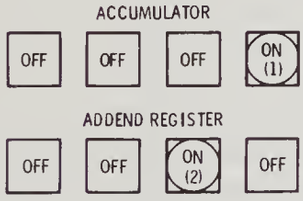


(C) Binary number 1 transferred into accumulator and addend register cleared.

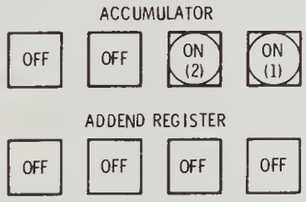
Fig. 3-2. Operation of accumulator and addend register.



(A) Binary 1 displayed by accumulator.



(B) Binary 2 entered into addend register.



(C) Binary 2 transferred to accumulator; binary 3 is displayed by accumulator, and addend register is cleared.

Fig. 3-3. Process of binary addition.

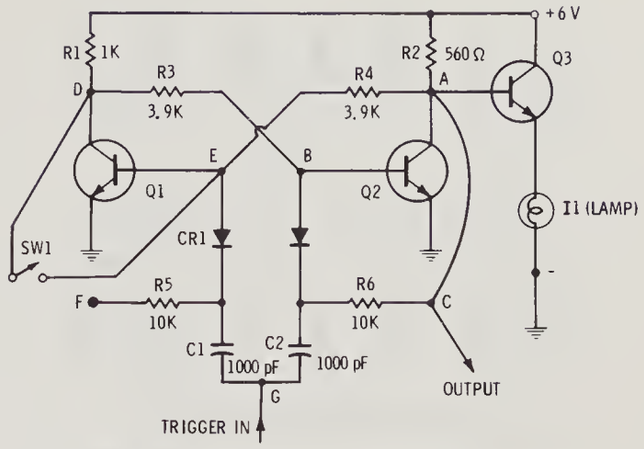


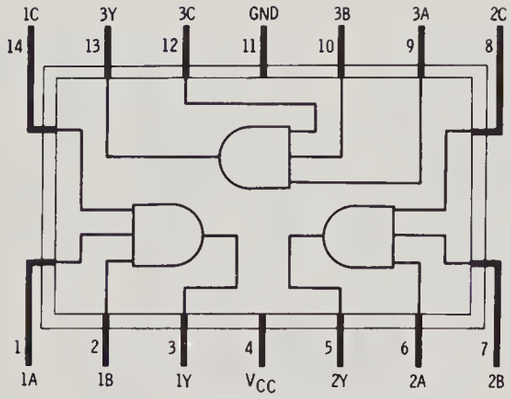
Fig. 3-4. Configuration of the halt command flip-flop.

number may be added into the accumulator by repeating the above procedure.

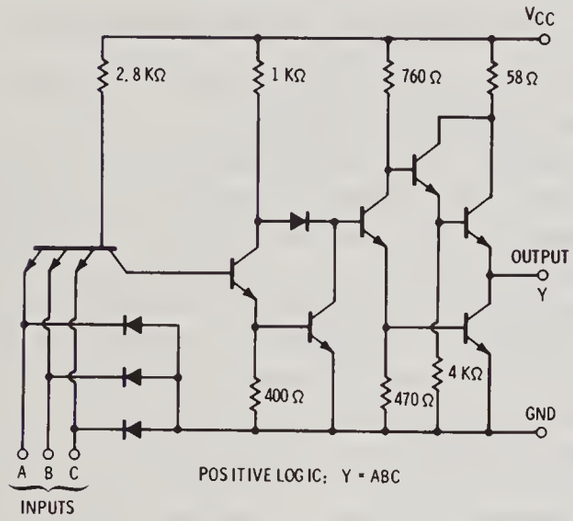
After the final sum has been stored in the accumulator, we proceed to clear the accumulator as follows. In the example of Fig. 3-3C, flip-flop lamps (2) and (1) must be turned off to clear the accumulator. These lamps are controlled by flip-flops A1 and A2 in Fig. 3-1. To turn the lamps off, we momentarily connect terminals A and B together on A2 and A1. In turn, the A1 and A2 indicator lamps stop glowing. The accumulator is thereby cleared, and the addend register may be programmed again, if desired. Here, it is instructive to note how the halt command flip-flop in Fig. 3-1 operates when Sw1 is closed and when it is opened. With reference to Fig. 3-4, observe that when Sw1 is closed, transistor Q1 must conduct because its base is biased positively. In turn, transistor Q2 is driven into cutoff. When Sw1 is then opened, the flip-flop remains in this state. Since CR2 is reverse-biased via R6, an applied trigger pulse at terminal G cannot flow into the base of Q2. On the other hand, the "0" level trigger pulse can flow through CR1 to the base of Q1 and drive it into cutoff. In turn, Q1 drives Q2 into conduction. In this state, terminal A is practically at ground potential, so that Q2 short-circuits the clock pulses to ground. Thus, the halt command stops the clock. To start the clock once more, we momentarily connect terminals D and E together (Fig. 3-4), which reverses the state of the halt flip-flop.

IC PACKAGE ARRANGEMENTS

Numerous digital IC package arrangements are encountered in digital-equipment servicing pro-



(A) Layout and terminal arrangement.



(B) Internal gate circuitry.

A	B	C	Y
1	1	1	1
1	1	0	0
1	0	1	0
1	0	0	0
0	1	1	0
0	1	0	0
0	0	1	0
0	0	0	0

(C) Truth table.

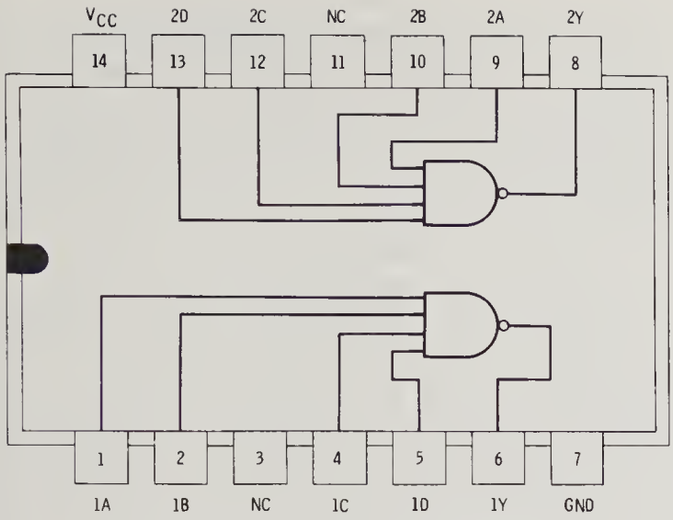
Fig. 3-5. A triple 3-input AND gate in a flat digital IC package.

cedures. For example, referring to Fig. 3-5, three AND gates are typically contained in a triple 3-input flat package, as shown in Fig. 3-5A. Each AND gate employs the circuit in Fig. 3-5B. Troubleshooting procedures, of course, are not directly concerned with the internal circuit details. Instead, the technician determines only if a normal output is obtained in response to normal input(s). This is an example of positive logic because the AND gate circuitry provides a positive output level for a binary 1, and a zero output level for a binary 0. This is sometimes stated in an equivalent way: positive logic provides a positive *true* level and a zero-volt *false* level. The note Y = ABC in Fig. 3-5B means that if all three inputs are pulsed positively, a positive output pulse will be obtained. If only one input or only two inputs are pulsed positively, there is no output from the AND gate. Or, if negative inputs are applied, there is no output from the AND gate.

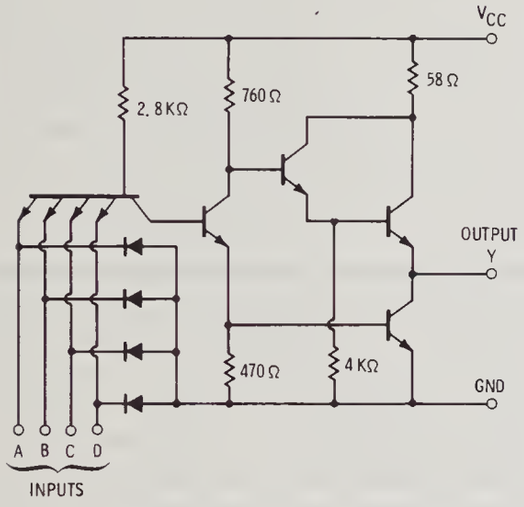
The foregoing logic facts are summarized by means of the truth table shown in Fig. 3-5C. Each of the AND gates in Fig. 3-5A has three inputs, identified as 1A, 1B, 1C; 2A, 2B, 2C; and 3A, 3B, 3C. In turn, the columns of the truth table are headed A, B, and C. This truth table states that if inputs A, B, and C are all logic-high (pulsed positively), the output Y will also be logic-high (binary 1). Next, if inputs A and B are logic-high, but input C is logic-low, the output Y will be logic-low (binary 0). Similarly, if inputs A and C are logic-high, but input B is logic-low, the output Y will be logic-low. In summary, the truth table states that a binary 1 output will be obtained only if all three inputs are at binary-1 level at the same time. A truth table is defined as a logic function that lists all possible combinations of input values and indicates the true output values for each input combination.

Next, Fig. 3-6 depicts dual 4-input positive NAND gates in an in-line IC package. Also shown are the schematic diagram for the internal circuitry of each gate and the corresponding truth table. Note that if all inputs are logic-high, the output is logic low. Any combination of logic-high and logic-low inputs results in a logic-high output. The note $Y = \overline{ABCD}$ in Fig. 3-6B means that the output Y is a binary 0, provided that all inputs are binary 1 at the same time. As noted previously, a bar over a letter has the significance of NOT. Another example of digital IC packaging is shown in Fig. 3-7. This is a quadruple 2-input positive NOR gate in a flat-package arrangement. The note $Y = \overline{A + B}$ means that the output Y is a binary 1, provided that both inputs are binary 0 at the same time, as seen in the truth table. Observe that the plus sign in the foregoing expression does not mean that the terms are added together. This is a special digital logic symbol which is explained in detail, along with other special digital logic symbols, in a following chapter.

Next, it is instructive to consider the hex inverter flat-package IV depicted in Fig. 3-8. *Hex* means that six inverters are contained in the package. The inverter circuit has one input and



(A)Layout and terminal arrangement.



NOTES: 1. COMPONENT VALUES SHOWN ARE NOMINAL
2. NC - NO INTERNAL CONNECTION

POSITIVE LOGIC: $Y = \overline{ABCD}$

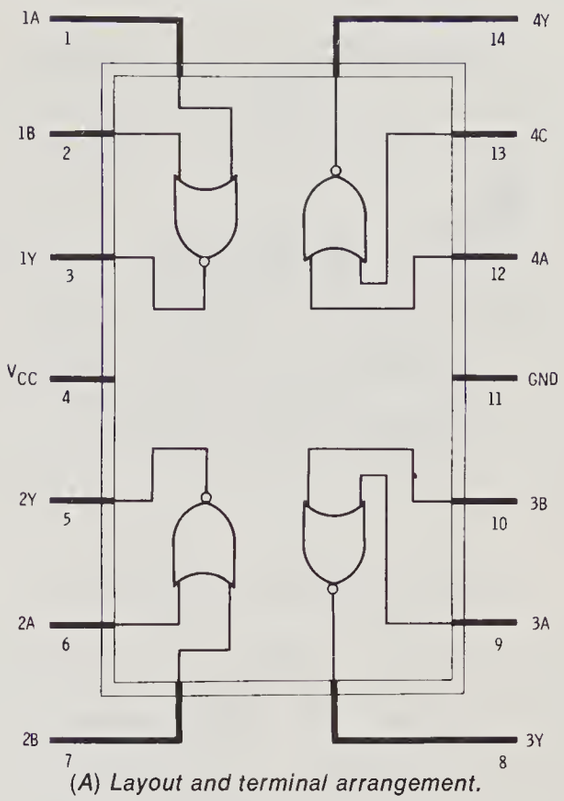
(B) Internal gate circuitry.

(C) Truth table.

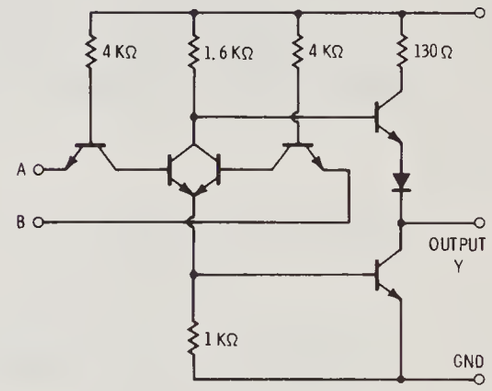
A	B	C	D	Y
1	1	1	1	0
1	1	1	0	1
1	1	0	1	1
1	0	1	1	1
0	1	1	1	1
0	0	1	1	1
0	0	0	1	1
0	1	1	0	1
1	0	0	1	1
0	1	0	0	1
0	0	1	0	1
0	0	0	0	1

Fig. 3-6. A dual 4-input positive NAND gate IC in an in-line package.

one output. It is a simple amplifier arrangement that inverts the input signal. When the input is logic-high, the output is logic-low, and vice versa. An inverter is also called a NOT circuit because it



(A) Layout and terminal arrangement.



POSITIVE LOGIC: $Y = \overline{A + B}$

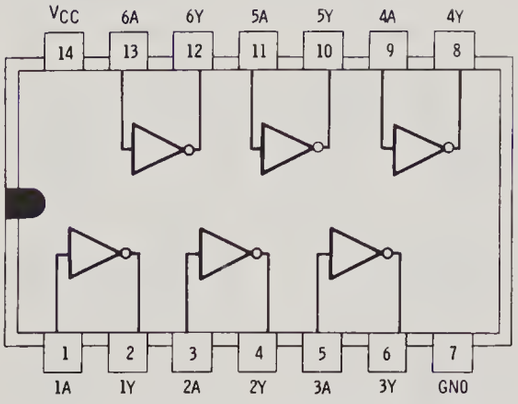
(B) Internal gate circuitry.

(C) Truth table.

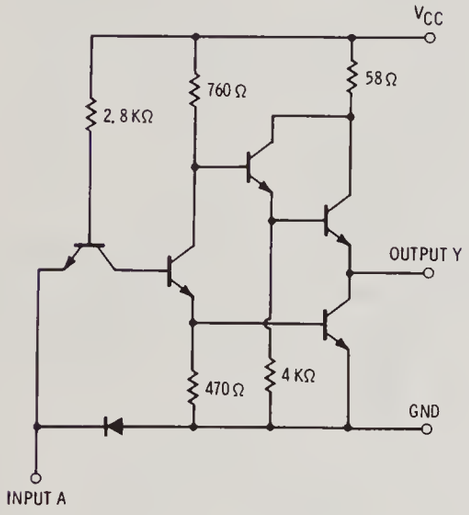
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Fig. 3-7. A quadruple 2-input positive NOR gate IC in a flat package.

reverses the input signal, as seen in the accompanying truth table. It is evident that if an AND gate is followed by an inverter, it becomes a NAND gate. Again, if an OR gate is followed by an inverter, it becomes a NOR gate. Note that a triangle symbol means an amplifier; a triangle symbol followed by a small circle means an inverting amplifier.



(A) Layout and terminal package.



(B) Internal inverter circuitry.

A	Y
0	1
1	0

(C) Truth table.

Fig. 3-8. A hex inverter IC in a flat package.

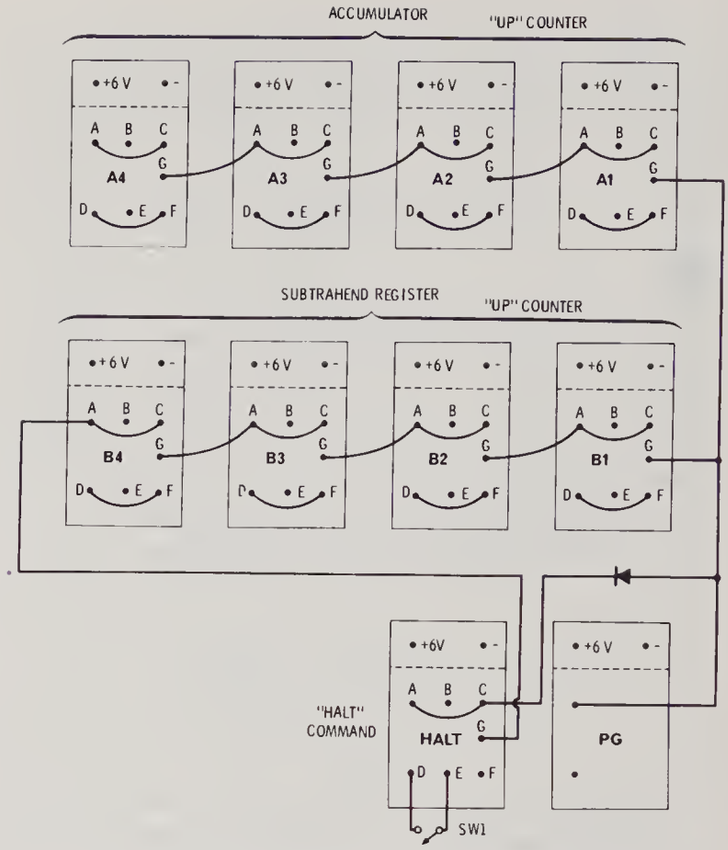


Fig. 3-9. Arrangement of a nongated binary subtractor.

NONGATED BINARY SUBTRACTER

A simple nongated binary subtracter is shown in Fig. 3-9. Note that its arrangement is somewhat the same as that of the nongated binary adder shown in Fig. 3-1. However, both the upper and the lower registers are up counters in a binary subtracter. Note that the lower register is called a *subtrahend* register and the upper register is still called the accumulator. To subtract a pair of binary numbers, enter the first number into the accumulator. This is accomplished by momentarily connecting together terminals D and E of the appropriate flip-flops in the accumulator. Next, enter the number to be subtracted into the subtrahend register, in the same manner. Then, start the subtraction process by momentarily closing Sw1 on the halt flip-flop. The clock will start and continue until the subtrahend register is cleared. The answer then appears in the accumulator register. If desired, a third binary number can be subtracted from the answer by repeating the preceding process. To finally clear the accumulator register, momentarily connect terminals A and B together on each flip-flop that displays a glowing lamp.

BINARY-CODED DECIMAL (BCD) COUNTER

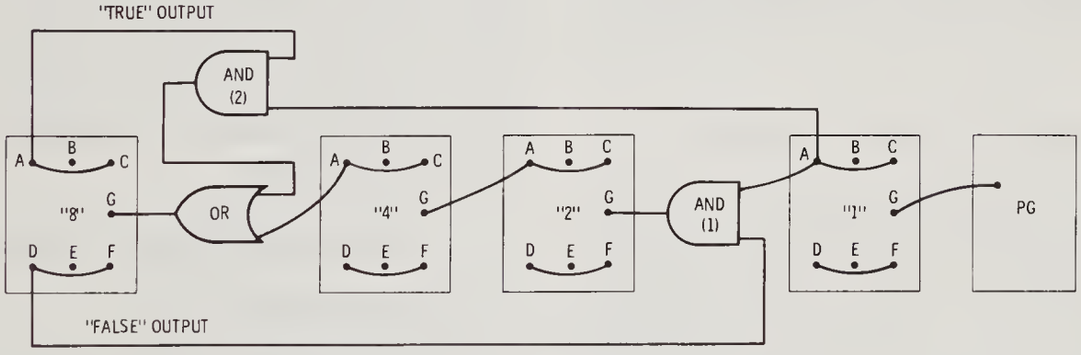
You will encounter many examples of binary-coded decimal (bcd) counters in digital servicing procedures. A bcd counter exemplifies a very basic application of logic gates in the production of decimal number readouts from binary numbers. A bcd counter employs four binary flip-flops to count to 10, as illustrated in Fig. 3-10. Two AND gates and an OR gate are used with four flip-flops and a pulse generator. Gate action causes the counting sequence to proceed: 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, and reset to 0000. With the bcd counter reset to 0000,

the FALSE output of the "8" flip-flop is on (high), since this flip-flop displays a "0." Therefore, when the "1" flip-flop is triggered on with a pulse from the clock, AND gate (1) has both inputs on, and the counter displays 0001. The AND gate is now ON, and the next clock pulse turns the "1" flip-flop off. As AND gate (1) turns off, it triggers the "2" flip-flop on. Accordingly, the counter display is now 0010. Next, the clock turns the "1" flip-flop on again, and the counter displays 0011. The AND gate is now on. Then, the next clock pulse turns the "1" flip-flop off again, and AND gate (1) switches off, turning off the "2" flip-flop. In turn, the "4" flip-flop is triggered on, and the counter display is 0100. Thus, a total of four pulses have been counted.

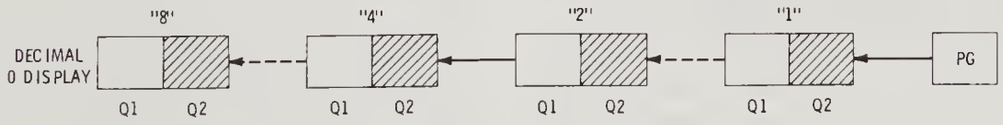
Note that the "4" flip-flop in Fig. 3-10 drives the OR gate, which is now on, inasmuch as one of the gate inputs is on. The previous circuit actions are repeated, producing displays of 0101, 0110, and 0111. Then, the eighth clock pulse resets the "1," "2," and "4" flip-flops to "0." Observe that when the "4" flip-flop is reset to "0," the OR gate is turned off and the "8" flip-flop is triggered, producing a counter display of 1000. At this point, the system is in a different state. In other words, the "8" flip-flop is now ON, and the FALSE output to AND gate (1) is now off. This means that AND gate (1) cannot be on while the "8" flip-flop displays a binary "1." When the next clock pulse occurs, the counter displays 1001. At this time, AND gate (2) has both inputs on, causing the gate to turn on. Consequently, an on (high) input is applied to the OR gate, and turns the gate on. Then, the next clock pulse resets the "1" flip-flop to "0," turning AND gate (2) off, which turns off the OR gate and produces a trigger pulse that resets the "8" flip-flop to "0." Thus, the counter displays 0000, and ten pulses have been counted.

IN-CIRCUIT TRANSISTOR TESTER

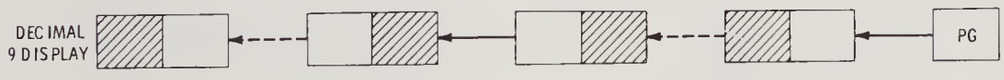
Troubleshooting of counter circuitry often involves transistor testing. Technicians may use an in-circuit transistor tester such as that shown in Fig. 3-11 for preliminary checking. This instrument provides go/no-go (good/bad) type of in-circuit test, which will often save the time used unsoldering transistor leads for an out-of-circuit test or a substitution test. Diodes can also be



(A) Logic diagram for counter.



(B) Decimal 0 display (also normal decimal 10 display).



(C) Decimal 9 display.

(D) Incorrect display 15; indicates hang-up trouble.

Fig. 3-10. A binary coded decimal (bcd) counter arrangement.

Courtesy, Heath Co.

Fig. 3-11. An in-circuit transistor tester.

checked in-circuit for good, shorted, or open conditions. In case of doubt, semiconductor devices can be unsoldered from their printed-circuit boards and tested out-of-circuit. The tester shown in Fig. 3-11 also provides transistor leakage tests and beta measurements. It is battery powered, and uses the circuit shown in Fig. 3-12. In-circuit tests are meaningful unless a semiconductor device is shunted by a very low value of circuit resistance.

NON-"HANG-UP" BCD COUNTER

Although the bcd counter depicted in Fig. 3-10 is comparatively simple, it has the disadvantage of possible "hang-up." In other words, if an erroneous display should occur for any reason, the OR gate may hang up and never turn off. Thus, if a display such as 1100, 1101, 1110, or 1111 happens to take place, a hang-up trouble symptom appears. To eliminate the possibility of hang-up, another AND gate can be included in the arrangement, as shown in Fig. 3-13. In case of an erroneous display, the additional AND gate permits continuation of counting, followed by reset, after which counting resumes in the correct BCD sequence.

LOGIC FAMILIES

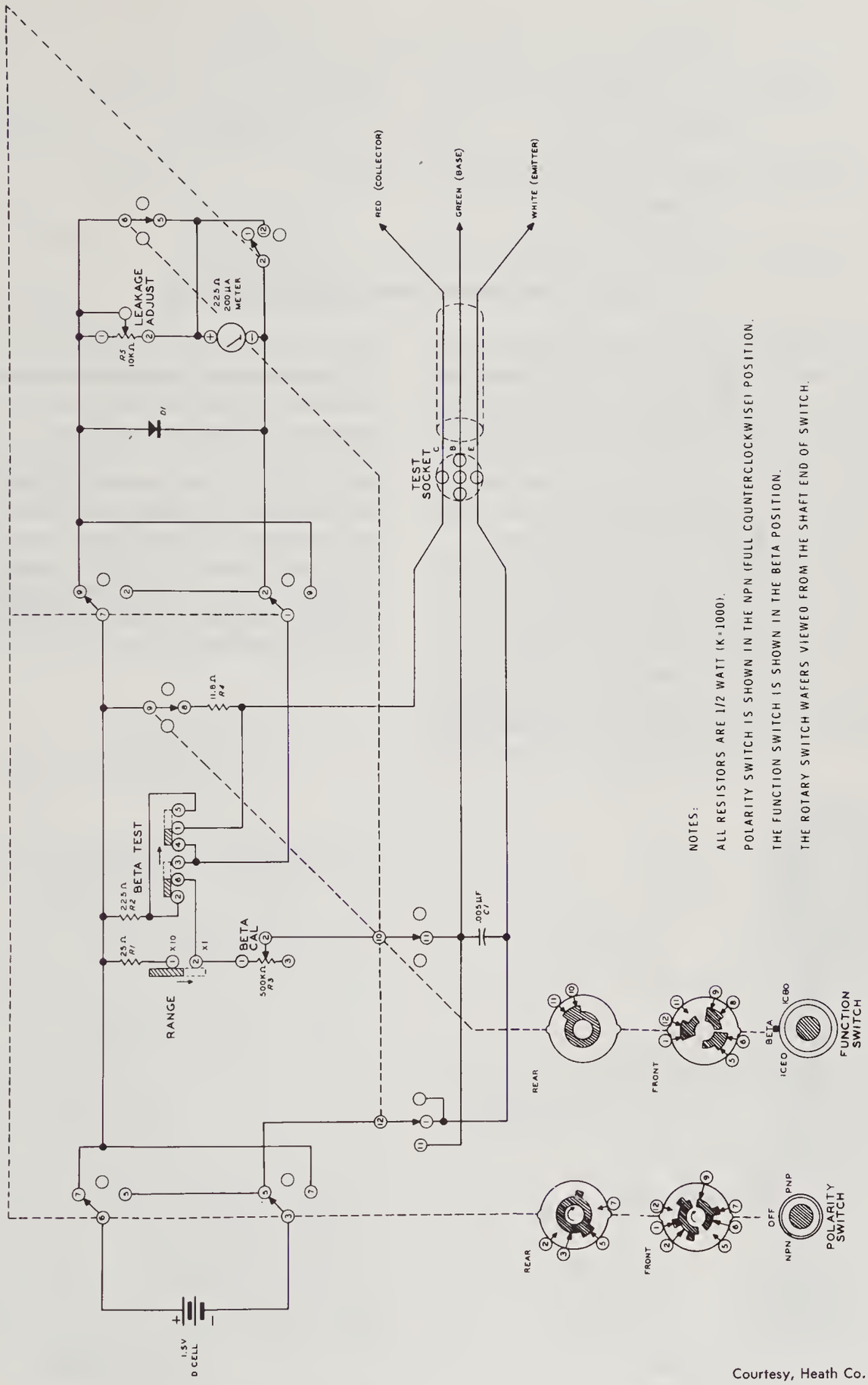
In servicing digital equipment, we encounter various logic families. A logic family employs specified kinds of components in the basic gate circuits within that family. Although each family provides gate circuits that function in the same way, different logic families have various advantages and disadvantages. Voltages, currents, and impedances are not necessarily the same from one logic family to another. Referring to Fig. 3-14, RTL (resistor-transistor logic) utilizes resistors to perform the logic operation, and a transistor to invert the input. An RTL gate performs the NOR function. A supply voltage of 3.6 volts is standard and positive logic is employed. The logic-high level is approximately 1 volt; the logic-low level is less than 0.4 volt. The logic-high level corresponds to a binary 1; the logic-low level corresponds to a binary 0.

An RTL dual 3-input NOR gate is shown in Fig. 3-15. Basically, only NOR gates exist in the RTL family. However, all of the logic operations can be performed by supplementing NOR gates. For example, Fig. 3-16 shows how a NOR gate can be followed by an inverter to provide the OR function. Next, if a NOR gate is preceded by a pair of inverters, as depicted in Fig. 3-17, the AND function is provided. Again, if a NOR gate is both preceded and followed by inverters, as seen in Fig. 3-18, the NAND function is provided. Digital equipment often employs quad inverters, such as those shown in Fig. 3-19, to supplement NOR gates. As a practical note, the RTL family is becoming less widely used and the technician is more likely to encounter various other logic families, as explained in the next chapter.

TROUBLESHOOTING TECHNIQUES

1. Incorrect Readout

When incorrect readout occurs, the technician makes tests to answer such questions as "Is a gate functioning?"; "Is a pin shorted to ground or Vcc"; and "Is a counter counting?" By using the proper test instruments, these tests can be made without unsoldering IC pins or cutting circuit-board conductors. A logic probe, as illustrated in Fig. 3-20, is generally regarded as the single most important test instrument that is used in digital-equipment troubleshooting. The probe is used to trace logic levels and pulses through integrated circuity in order to determine whether the point under test is logic-high, logic-low, bad level, open-circuited, or pulsing. This probe has preset logic threshold levels of 2.0 volts (logic-high) and 0.8 (logic-low) volt. When the logic probe is applied at a high-level terminal, a bright band of light



Courtesy, Heath Co.

Fig. 3-12. Circuit for the transistor tester shown in Fig. 3-11.

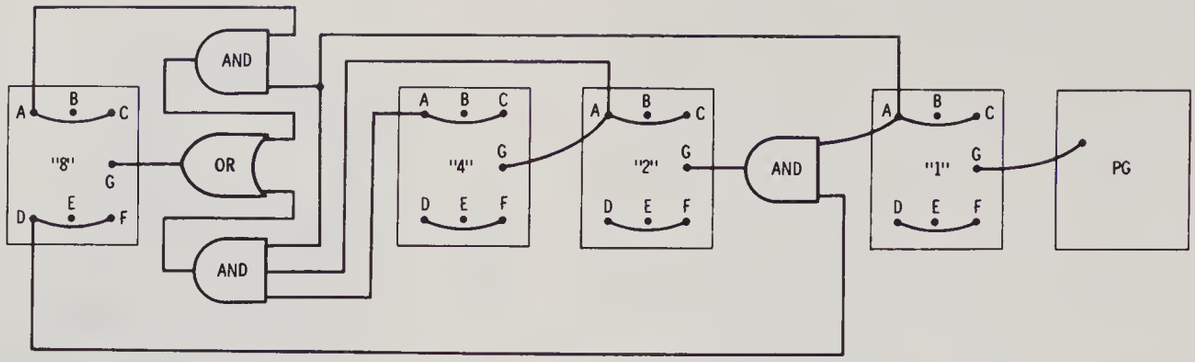
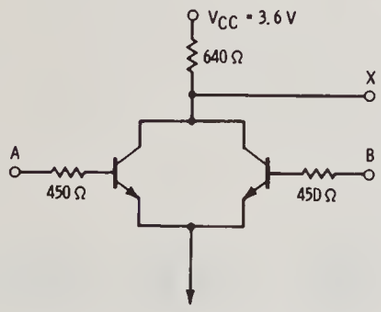


Fig. 3-13. A non "hang-up" binary-coded decimal counter.

appears around the probe tip. On the other hand, when the probe is touched to a low-level terminal, the light goes out. Open circuits or "bad-level" voltages produce illumination at half brightness. The lamp flashes on or blinks off, depending on the polarity of the pulse. To facilitate evaluation, pulse trains up to 50-MHz repetition rate cause the lamp to blink on and off at a 10-Hz rate.

To determine whether pulse trains may be missing, a logic probe can be applied at various test points while the circuit is run at normal speed. Next, for more exacting tests, the circuit can be stepped one pulse at a time while checking the truth tables of the logic packages. For this purpose, a single-shot pulse generator is required. For example, a logic pulser, such as that illustrated in Fig. 3-21, is very convenient for this purpose. Probe and pulser operation is automatic, and no adjustments are provided. This is a practical advantage, in that the technician is free to devote his attention to circuit analysis instead of being distracted by instrument adjustments. Connectors used with the logic probe and pulser provide connection to a 5-volt power supply either from the circuit under test or from a service-type power supply. A ground clip is used to connect the probe circuitry to the ground or common bus of the circuit under test.



(A) Typical NOR circuit.

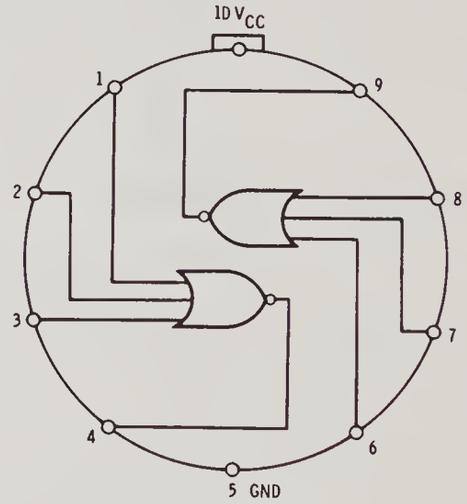
(B) NOR gate symbol.

A	B	X
H	H	L
L	H	L
H	L	L
L	L	H

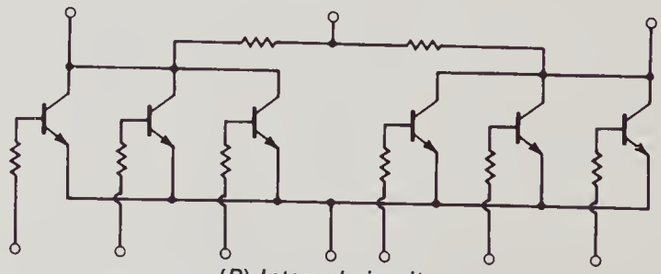
A	B	X
1	1	D
D	1	D
1	D	D
D	0	1

(C) Truth table.

Fig. 3-14. Basic RTL logic.



(A) Logic symbol.



(B) Internal circuitry.

Fig. 3-15. Example of an RTL dual 3-input NOR gate.

(A) NOR gate symbol.

A	B	X
0	0	1
0	1	0
1	0	0
1	1	0

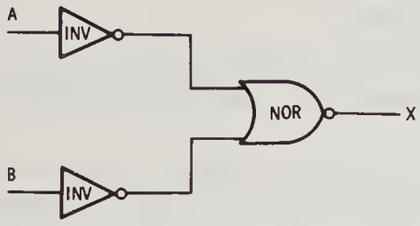
(B) NOR gate truth table.

(C) NOR gate followed by inverter to form an OR gate.

A	B	X
0	0	0
0	1	1
1	0	1
1	1	1

(D) OR gate truth table.

Fig. 3-16. NOR gate and an inverter form an OR gate.

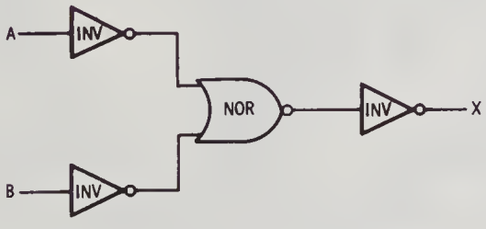


(A) NOR gate and inverter arrangement.

(B) AND gate truth table.

A	B	X
0	0	0
0	1	0
1	0	0
1	1	1

Fig. 3-17. NOR gate with inverters at the inputs form an AND gate.

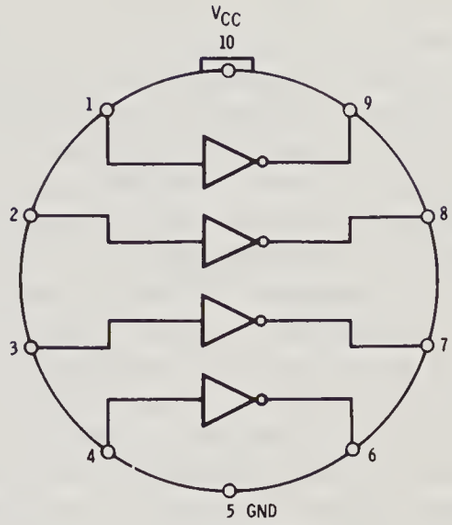


(A) NOR gate and inverter arrangement.

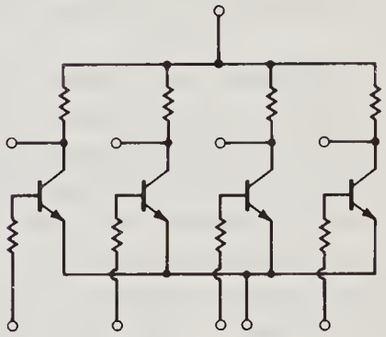
(B) NAND gate truth table.

A	B	X
0	0	1
0	1	1
1	0	1
1	1	0

Fig. 3-18. NOR gate with inverters at the inputs and output form a NAND gate.



(A) Logic diagram.



(B) Schematic.

Fig. 3-19. A quad inverter.

Fig. 3-20. A logic probe for troubleshooting digital circuitry.

Courtesy, Hewlett-Packard

An example of pulser and logic probe application is illustrated in Fig. 3-22. The pulser tip is touched to the input test terminal, and the pulse button is pressed. In turn, all of the circuits connected to the terminal are briefly driven to their opposite state. In turn, the logic probe indicates the resulting response (or lack of response) at the output test terminal. Note that the technician does not need to determine whether the points under test are in logic-high or logic-low states. In other words, the pulser action is automatic; each time that the pulser button is pressed, high nodes are pulsed low and low nodes are pulsed high. (A node is a terminal of any branch of a network.) The logic pulser can provide a drive current up to 0.65 ampere; its output pulse width is 0.3μs, which ensures that the total driving energy is sufficiently small that semiconductor devices will not be damaged.

Logic-probe response to different inputs is depicted in Fig. 3-23. Positive pulses with widths of 25 ns or greater are stretched to 0.1-second width, and cause the indicator light to glow for 0.1 second. Negative pulses will cause the indicator light to be momentarily extinguished. High-frequency pulse trains cause partial illumination of the indicator lamp. A wide pulse will cause the light to glow as long as the pulse occurs. Also shown in Fig. 3-23 is a block diagram for the logic probe. Both the input circuit and the power supply are provided with overvoltage protection. Note that the threshold discriminator and input amplifier serve to set the threshold at approximately 1.4 volts. Two pulse stretchers follow the input amplifier, one of which will automatically trigger on each incoming pulse, in accordance with pulse polarity. Each of these pulse stretchers consists of a monostable multivibrator; while one of them inverts, the other stretches the incoming pulse. In turn, the output from the second stretcher drives the indicator lamp by means of a transistor switch.

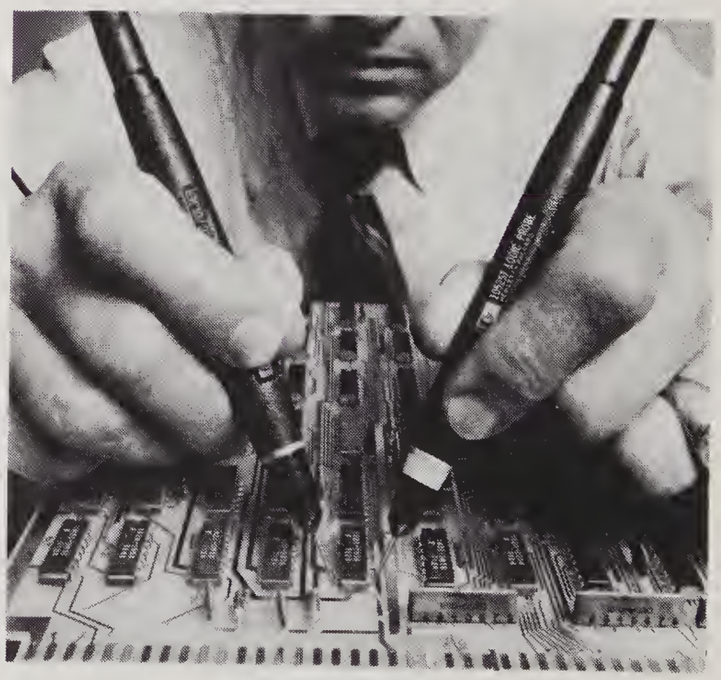
2. No Readout

A no-readout trouble symptom may be caused by one or more of the following faults:

a. Vcc (supply voltage) short-circuited to ground (measure the supply voltage).
b. Clock pulses absent; check for open circuit, such as a broken circuit-board conductor.
c. IC "popped out" of its socket.
d. Module not fully inserted into its receptacle.
e. Incorrect replacement circuit board.

Courtesy, Hewlett-Packard

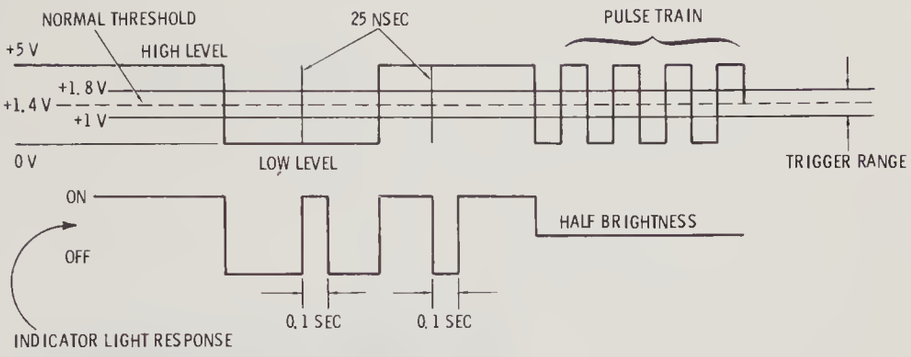
Fig. 3-21. A logic pulser type of single-shot pulse generator.



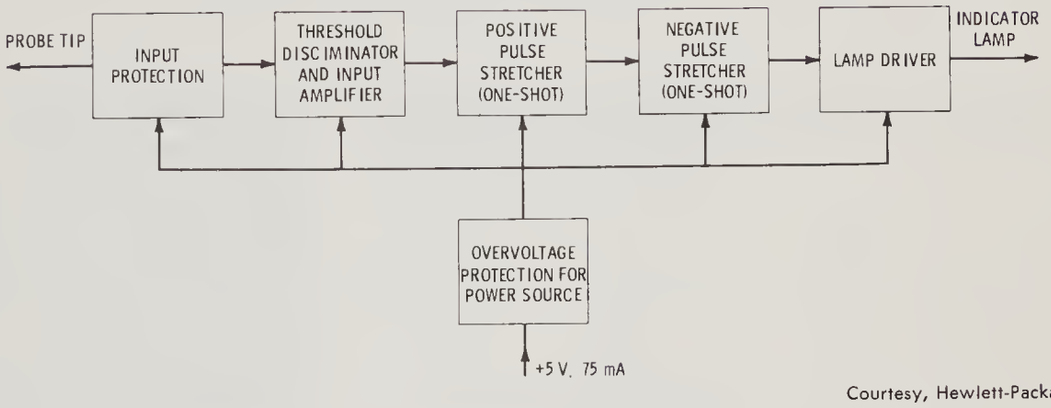
Courtesy, Hewlett-Packard

Fig. 3-22. Example of logic pulse and probe application.

(A) Response to different inputs.



(B) Block diagram of probe.



Courtesy, Hewlett-Packard

Fig. 3-23. Digital logic probe arrangement.

3. Erratic Operation

Erratic operation can be caused by either mechanical or electrical defects. When this trouble symptom appears, signal-tracing procedures with a logic probe or an oscilloscope will usually localize the defective section of the equipment. Possible causes of erratic operation are as follows:

a. Corroded or damaged contacts on the module.
b. Cold-soldered connection.
c. Defective or corroded contacts in the IC socket.
d. High ripple on power-supply bus.
e. Fluctuating power-supply voltage.

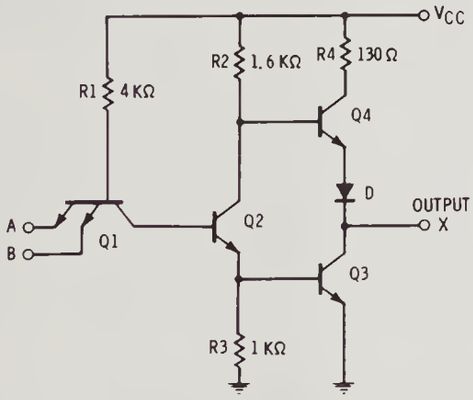
4. Malfunction On Large Numbers Only

When an adder, subtracter, or bcd counter develops malfunction(s) on large numbers only, preliminary localization of the defective section can usually be made by evaluating the block diagram of the digital equipment. In other words, the trouble will be found in a branch circuit that connects between the malfunctioning portion of the equipment and the normally operating portion. As a simple example, if the bcd counter in Fig. 3-10 overflows, displays a decimal 11 and hangs up, the OR gate would fall under preliminary suspicion. In turn, its response can be quickly checked out with a logic pulser and probe. If the OR gate is cleared from suspicion, the "8" flip-flop would be tested next. However, the "4" flip-flop would be disregarded. That is, all of the circuitry up to and including the "4" flip-flop would be assumed to be functioning normally.

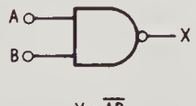
CHAPTER 4

Gates and Associated Equipment

As noted previously, the digital technician encounters various families of logic. One of the most widely employed families is called transistor-transistor logic (TTL or T^2L). In some data sources, TTL is also referred to as multiemitter transistor logic. A distinctive feature of TTL is the use of a multiple emitter transistor instead of diode inputs, as seen in Fig. 4-1. In other words, a 4-input TTL gate will utilize four emitters in a single transistor for the inputs. The NAND gate depicted in Fig. 4-1 is a positive-level device employing the npn transistor, Q1. A 5-volt power supply is standard for TTL circuitry. A logic-high level of 2 volts and a logic-low level of 0.8 volt are typical. Fig. 4-2 shows an 8-input TTL NAND gate.



(A) Internal circuitry.



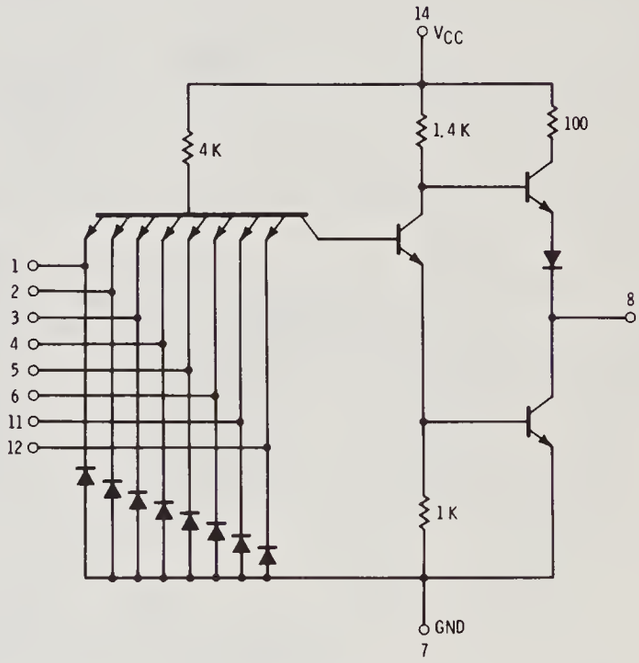
(B) Logic symbol.

$X = \overline{AB}$

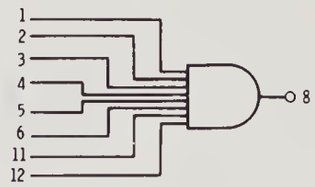
Courtesy, General Electric

Fig. 4-1. Example of a 2-input TTL gate.

Common trouble symptoms caused by faults in TTL digital systems are:



(A) Internal circuitry of IC.



POSITIVE LOGIC:

$8 = \overline{1 \cdot 2 \cdot 3 \cdot 4 \cdot 5 \cdot 6 \cdot 11 \cdot 12}$

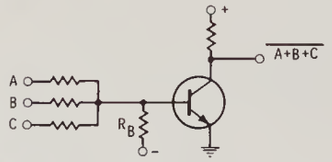
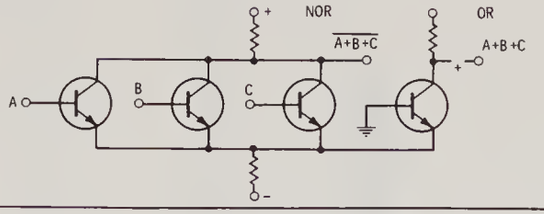
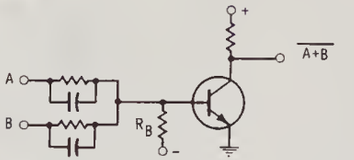
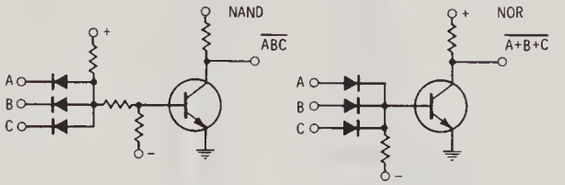
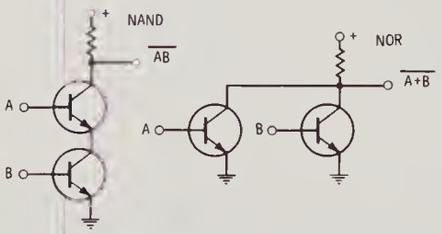
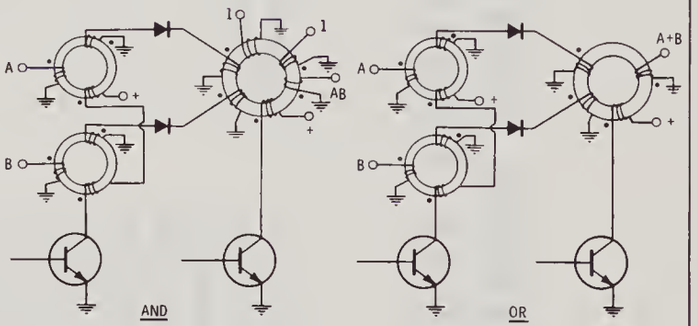
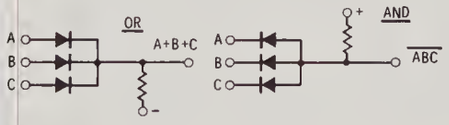
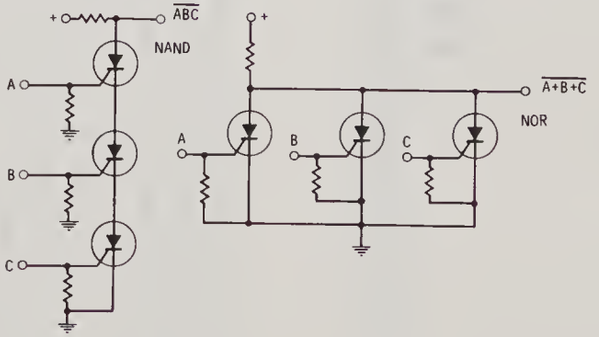
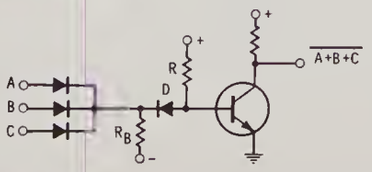
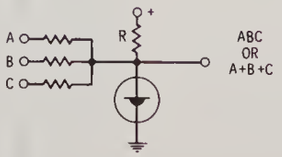
NEGATIVE LOGIC:

$8 = \overline{1 + 2 + 3 + 4 + 5 + 6 + 11 + 12}$

(B) Logic symbol and terminal identification.

Fig. 4-2. Arrangement of an 8-input TTL NAND gate.

Table 4-1. Common Logic Systems

NAME	TYPICAL CIRCUIT (Positive signals are defined as 1)	DESCRIPTION	NAME	TYPICAL CIRCUIT (Positive signals are defined as 1)	DESCRIPTION
RTL Resistor-transistor logic (NOR)		Logic is performed by resistors. Any positive input produces an inverted output irrespective of the other inputs. Resistor R_B gives temperature stability.	**CML** Current-mode logic		Logic is performed by transistors which are biased from constant current sources to keep them far out of saturation. Both inverted and noninverted outputs are available.
RCTL Resistor-capacitor-transistor logic (NOR)		Same as RTL except that capacitors are used to enhance switching speed. The capacitors increase the base current for fast collector current turn on and minimize storage time by supplying a charge equal to the stored base charge.	**DTL** Diode transistor logic		Logic is performed by diodes. The output is inverted. The transistor acts as an amplifier. This is essentially an extension of diode logic.
DCTL Direct-coupled transistor logic		Logic is performed by transistors. V_{CE} and V_{BE} measured with the transistor in saturation, define the two logic levels. V_{CE} must be much less than V_{BE} to ensure stability and circuit flexibility.	**CDL** Core-diode logic		Logic is performed by cores and transmitted by diodes. Transistors act as drivers to shift information. Each transistor can drive many cores but not successive cores in the logic line.
DL Diode logic		Logic is performed by diodes. The output is not inverted. Amplifiers are required to maintain the correct logic levels through several gates in series.	**4-Layer** Device logic		Logic is performed by silicon controlled switches which are triggered on at the gate lead. The gates can be actuated by pulse or dc levels. The gates have a built in memory and must be reset.
LLL Low-level logic (NOR)		Logic is performed by diodes. The output is inverted. The diode D isolates the transistor from the gate permitting R to turn on the collector current. This method is also called current switching diode logic.	**TDL** Tunnel-diode logic		Logic is performed by tunnel diode switching from low voltage to high voltage state. Whether circuit represents AND or OR gate depends on bias current through resistor R. Tunnel diode biased near peak current for OR gate, and close to ground for AND.

1. "Stuck-at" condition.
2. Pulse dropouts.
3. Aliasing or introduction of spurious pulses.
4. Intermittent operation.

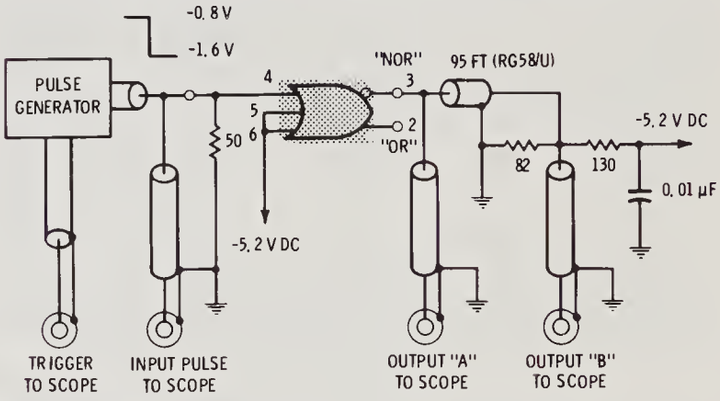
BASIC LOGIC FAMILIES

With reference to Table 4-1, it is helpful to note briefly the common logic systems that are tabulated. The resistor-transistor logic (RTL) discussed in the preceding chapters has a typical power-supply voltage of 3.6 volts. The logic-high level is approximately 1 volt, and the logic-low level is less than 0.4 volt. In addition to the RTL family, a variant called the mW RTL family is in use. This is the low-power resistor-transistor logic family. It employs a typical power-supply voltage of 3.6 volts but draws only 20% of the current demanded by a corresponding RTL configuration. Next, resistor-capacitor-transistor logic (RCTL) is essentially the same as RTL, except that capacitors are included to increase the speed of operation. It follows that an RTL device is not an equivalent replacement for an RCTL device, although it is practical to replace an RTL device with an RCTL device in various situations.

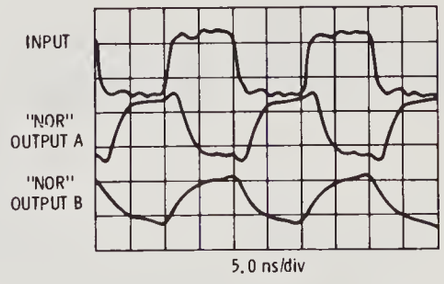
Direct-coupled transistor logic (DCTL) is not in extensive use, although the technician may encounter it occasionally in older digital equipment. It differs from RTL and RCTL in that logic operations are not performed by resistors, but by transistors. Direct-coupled transistor logic is so called because the input pulses are applied directly to the transistor bases. One of the trouble symptoms that can easily develop with DCTL is "current hogging." In this situation, the circuit drives several other DCTL NOR gates. If circuit tolerances drift, one of the base-emitter junctions will turn on before the others. In turn, the current demand of this turned-on junction may cause sufficient loading of the supply voltage that the other base-emitter junctions fail to turn on. For this reason, RTL is preferred since load-current demand is limited. Note that both NOT AND and NOT OR DCTL gates are depicted in Table 4-1.

Next, observe the diode logic (DL) arrangement depicted in Table 4-1. In this positive-logic arrangement, the diodes may be polarized either way. As indicated in the diagrams, one polarization provides an OR gate, whereas the other polarization provides an AND gate. Observe next that low-level logic (LLL) is a variation of RTL. This is a seldom-used system although it may be occasionally encountered in older designs. On the other hand, current-mode logic (CML), also called emitter-coupled logic (ECL), is in extensive use. A power-supply voltage of 5.2 volts is typical for ECL. It is instructive to observe the ECL NOR/OR gate line-driver test circuit shown in Fig. 4-3. Note that although the pulse generator applies a virtually perfect driving pulse to the gate, the output waveforms are substantially distorted. This distortion is normal in high-speed operation (50-MHz repetition rate in this example). In low-speed operation, however, the output waveform will appear practically the same as the input waveform. Note also that this is a positive-logic system in which the normal logic-high level is −0.8 volt, and the logic-low level is −1.6 volts. (Manufacturers are not entirely consistent on this definition of logic level. See the discussion under *Emitter-Coupled Logic Probe* at a later point in this chapter.)

Next, note that diode transistor logic (DTL) employs diode logic (DL) followed by an inverter. An inverter is an amplifier that reverses the input polarity. Digital amplifiers called buffers are also utilized to increase the available load power.



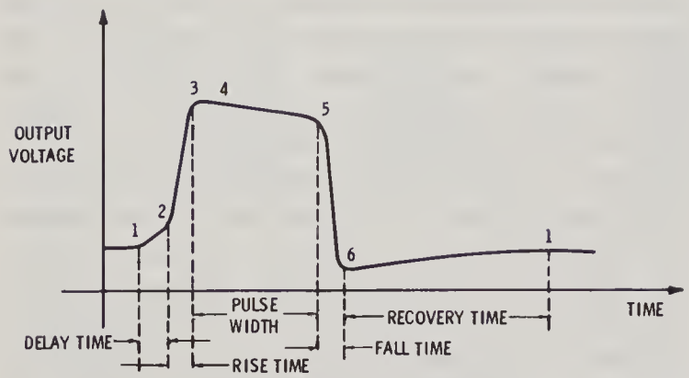
(A) Equipment connections.



Courtesy, Motorola Inc.

(B) Normal response at 50-MHz repetition rate.

Fig. 4-3. Line-driver test setup for typical ECL NOR/OR gate.



Courtesy, RCA

Fig. 4-4. Waveshape of a typical TDL digital pulse.

Note that the inverter used in the DTL circuit operates in class B and does not conduct until the transistor base is driven positive. DTL, which is in comparatively wide use, utilizes a typical power-supply voltage of 5 volts. Next, observe that core-diode logic (CDL) is considerably different from the aforementioned logic families. CDL utilizes electromagnetic induction and magnetic field storage. It is not used as extensively as various other families because its speed of operation is somewhat limited. Note that cores are basically high-reliability components and seldom fail. However, in case of malfunction, open or shorted connecting leads are primary suspects.

Comparatively heavy loads are accommodated by 4-layer diode logic. Power-supply voltages of 12, 18, and 24 volts are utilized in various designs. This type of logic is not in wide use. Similarly, tunnel-diode logic (TDL) is not often encountered by the digital technician. A tunnel diode operates at less than 1.0 volt, although the power-supply voltage is often much higher. The logic-high level is typically ±0.8 volt, and the logic-low level practically zero. Tunnel diodes can operate at very high speed; Fig. 4-4 shows the waveshape of a high-speed digital pulse from a tunnel-diode gate. Table 4-2 summarizes the typical operating characteristics of the logic families that have been noted.

As its name indicates, high-threshold logic (HTL) employs circuitry that responds to comparatively large logic-high levels. Accordingly,

Table 4-2. Typical Operating Characteristics of Logic Families in Extensive Use

Logic	Form	Delay (ms)	Freq of Flip-Flop (MHz)	Power Dissipation (mW)	Internal Noise	External Noise Immunity	Power-Supply Voltages
RTL	R_T	24	8	12	Fair	Fair	3 V ±10% and 3.6 V ±10%
mW RTL	R_T	45	1-3	2.5	Fair	Fair	3 V ±10% and 3.6 V ±10%
DTL	D_T	30	10	9	Fair	Good	4 V ±10%
VTL	D_T	50-60	1	12-80	Good	Excellent	±4 V to ±10 V
ECL	Current Mode	6	30	35	Excellent	Fair	4.2 V ±20%
TTL	T_T	10	20	15	Good	Good	5 V ±10%
HTL	D_T	200	3	45	Good	Excellent	18 V

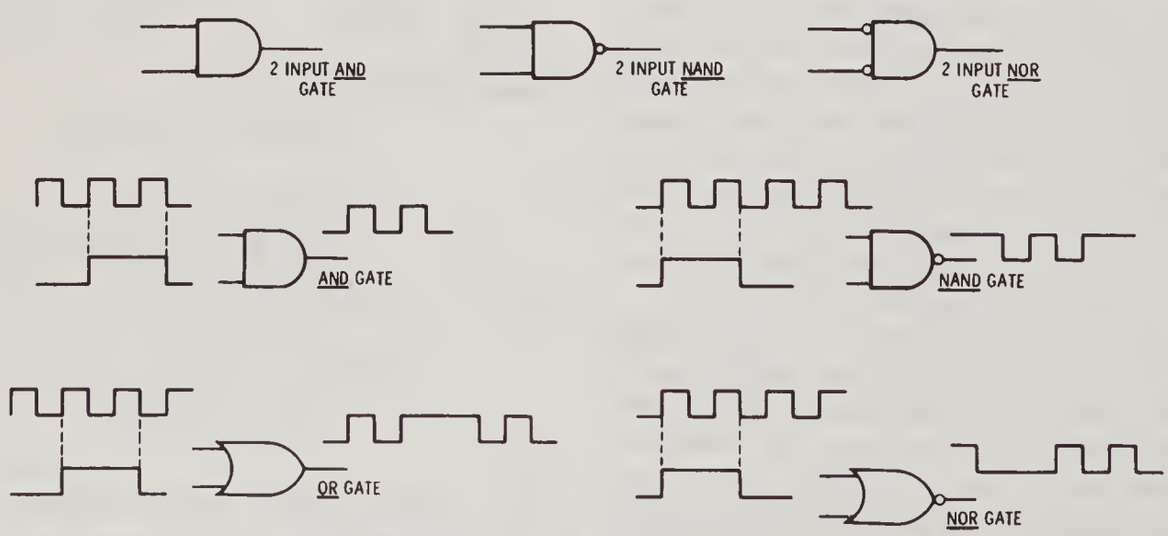


Fig. 4-5. Basic gate responses to a pair of input waveforms.

Courtesy, Hewlett-Packard

Fig. 4-6. A logic clip used in troubleshooting TTL or DTL ICs.

this system has better immunity to noise and is less likely to develop spurious responses in the presence of strong stray fields. A power-supply voltage of 18 volts is typical for HTL. Variable-threshold logic (VTL) is a variant of HTL that operates from power-supply voltages in the range from 8 to 20 volts. VTL also has superior immunity to noise, compared with various other logic families. Both HTL and VTL are basically diode transistor (DT) configurations. Note that the logic result is always the same, regardless of circuitry variations that may be employed. Fig. 4-5 presents a convenient summary of responses for 2-input AND, OR, NAND, and NOR gates.

The logic clip illustrated in Fig. 4-6 is a very useful instrument for troubleshooting TTL or DTL ICs. This tester clips onto the IC and instantly displays the logic states of all 14 or 16 terminals. Sixteen light-emitting diodes (LEDs) in the tester will independently follow level changes at each of the IC terminals. An illuminated LED indicates a logic-high state. The logic clip contains its own gating logic for locating ground and the +5-V supply terminals on the IC. Tests of sequential arrangements such as flip-flops are accomplished with the logic clip simultaneously monitoring all output states while the logic pulser is used to apply reset pulses to the flip-flop, as explained in greater detail subsequently. Faulty operation becomes immediately apparent because a defective IC will not go through its prescribed sequence of states.

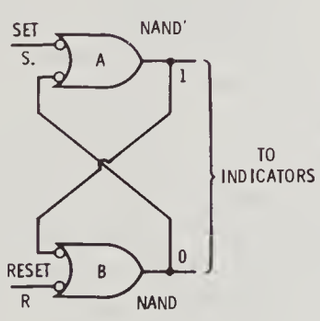
A logic clip can be used only with flat-pack ICs. However, a logic pulser and logic probe can be used to troubleshoot flat-pack ICs, transistor-case IC packages, and various discrete-component circuit boards. The clips, pulsers, and probes discussed here are useful only with TTL, DTL, and some other forms of logic that employ logic-high and logic-low levels in the vicinity of 2.0 and 0.8 volts. However, other types of logic probes are available, as will be explained later in this chapter. In any case, digital pulse generators, vom's, and oscilloscopes can be used for testing any type of logic.

BASIC FLIP-FLOP ARRANGEMENTS

At this point, it is helpful to consider the basic flip-flop arrangements that are encountered in digital servicing procedures. The reset-set (R-S) flip-flop is the simplest design and, as its name denotes, it has two inputs: a *set* input and a *reset* input. It has a "true" output and a "false" output, or binary 1 and 0 outputs. The meaning of the terms *set* and *reset* is evident from the following circuit actions:

1. If a logic-low pulse is applied to the set input, the flip-flop is driven to its 1 state.
2. If a logic-low pulse is applied to the *reset* input, the flip-flop is driven to its 0 state.

Fig. 4-7A shows a common type of R-S flip-flop consisting of a pair of NAND gates. Note that



(A) Configuration.

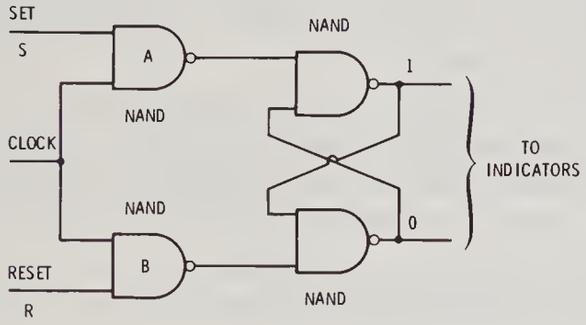
		(1)	(2)	(3)	(4)	(5)	(6)
		INITIAL CONDITIONS		PULSED LOGIC INPUTS		OUTPUT RESULT	
		1 OUTPUT	0 OUTPUT	SET INPUT	RESET INPUT	1 OUTPUT	0 OUTPUT
FLIP-FLOP IN "1" STATE INITIALLY	(1)	HI	LO	LO	LO	INDETERMINATE	
	(2)	HI	LO	LO	HI	HI	LO
	(3)	HI	LO	HI	LO	LO	HI
	(4)	HI	LO	HI	HI	HI	LO
FLIP-FLOP IN "0" STATE INITIALLY	(5)	LO	HI	LO	LO	INDETERMINATE	
	(6)	LO	HI	LO	HI	HI	LO
	(7)	LO	HI	HI	LO	LO	HI
	(8)	LO	HI	HI	HI	LO	HI

(B) Truth table.

Fig. 4-7. A basic R-S flip-flop.

an OR gate with inverted inputs becomes a NAND gate. Assume that the flip-flop is in its "1" state, with its 1 output logic-high and its 0 output logic-low; this condition accompanies logic-high set (S) and reset (R) inputs. Thus, gate A has a logic-high output which makes the upper input of gate B logic-high. Gate B has two logic-high inputs, and its output is logic-low. This logic-low from Gate B makes the lower input of gate A logic-low, producing a logic-high output from gate A. Note that the S and R inputs are both disabled when logic-high. Hence, gates A and B are "latched" in the logic-high state until the input levels are changed.

Observe in the truth table of Fig. 4-7B that when the flip-flop is initially in its "0" state, with its 1 output logic-low and its 0 output logic-high and with its S and R inputs logic-high, gate B is continuously enabled by gate A and gate A is continuously disabled by gate B. As before, this is a latched condition that continues until the input levels are changed. Now, if a logic-low pulse is applied to the S input, gate A will be enabled and will produce a logic-high pulse at its output. A logic-high pulse will also be applied to the upper input of gate B. In turn, gate B is disabled and its output becomes logic-low. Also, gate B enables the lower input of gate A, and the flip-flop is latched. Next, if a logic-low pulse is applied to the R input, gate B becomes enabled, gate A becomes disabled, and the flip-flop is latched.



(A) Configuration.

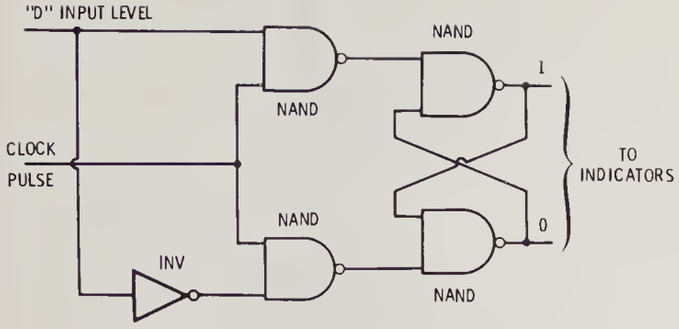
INITIAL CONDITIONS		LOGIC INPUT		AFTER CLOCK PULSE	
1 OUTPUT	0 OUTPUT	SET	RESET	1 OUTPUT	0 OUTPUT
LO	HI	LO	LO	LO	HI
LO	HI	LO	HI	LO	HI
LO	HI	HI	LO	HI	LO
LO	HI	HI	HI	INDETERMINATE	
HI	LO	LO	LO	HI	LO
HI	LO	LO	HI	LO	HI
HI	LO	HI	LO	HI	LO
HI	LO	HI	HI	INDETERMINATE	

(B) Truth table.

Fig. 4-8. Typical clocked R-S flip-flop.

An important fact to note is that when both inputs of an R-S flip-flop are simultaneously enabled by logic-low pulses, the flip-flop state will be indeterminate. In other words, this form of input could result in either a "1" output condition or a "0" output condition. Therefore, care must be observed in R-S flip-flop operation to ensure that both inputs are not simultaneously enabled by logic-low pulses. Cross-connected gates function as flip-flops because the gates have gain and the cross-connection provides positive feedback. Continuous oscillation does not occur because of direct coupling with resulting latch-up. However, change of state requires sufficient drive to more than cancel the prevailing feedback level. Note that change of state requires a logic-low input because input inversion then applies a logic-high input to the OR gate. Simultaneous logic-low inputs result in indeterminate outputs because logic-high inputs are then being applied to both OR gates, and cross-connection prevents both outputs from being logic-high at the same time. Simultaneous logic-high inputs have no effect on the existing state of the flip-flop, because the inverters apply logic-low levels to both OR gates which are unresponsive to logic-low inputs.

Next, consider the clocked R-S flip-flop shown in Fig. 4-8. In most equipment, the flip-flop inputs are first enabled (conditioned) and then driven into the specified change of state by a pulse from another source, such as a clock. Observe that the clocked R-S flip-flop in Fig. 4-8 is very similar to the R-S flip-flop described above. However, a steering network is also provided, which steers clock pulses to either set or reset the flip-flop. This steering network comprises a pair of 2-input NAND gates. The action of steering diodes was explained in Chapter 1. Note that when the set input is enabled with a logic-high level, NAND gate A will be enabled upon application of a logic-high clock pulse. In turn, gate A will apply a logic-low set pulse to the R-S flip-flop, and the flip-flop will change state to its "1" condition. On the other hand, when a logic-low level is applied to the set input and the reset input is enabled with a logic-high pulse, NAND gate B will be enabled upon application of a logic-high clock pulse. In turn, gate B will apply a logic-low reset pulse to the R-S flip-flop which then changes state to its "0" condition.



(A) Configuration.

INITIAL CONDITIONS		D INPUT LEVEL	AFTER CLOCK PULSE	
1 OUTPUT	0 OUTPUT		1 OUTPUT	0 OUTPUT
LO	HI	LO	LO	HI
HI	LO	LO	LO	HI
LO	HI	HI	HI	LO
HI	LO	HI	HI	LO

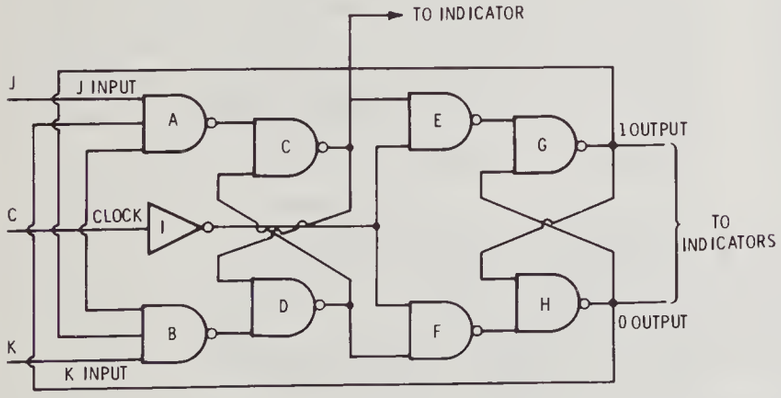
(B) Truth table.

Fig. 4-9. Typical D-type flip-flop.

To ensure that an indeterminate state does not occur in flip-flop operation, the D-type flip-flop is also utilized in digital equipment. A typical D-type flip-flop, which has one conditioning input called the data or D input, is shown in Fig. 4-9. In operation, the D input is either logic-high or logic-low. The level that is present at the D input will pass through to the 1 output when the leading edge of a clock pulse arrives at the clock input. In other words, if the D input is logic-high before and during a clock pulse, the flip-flop changes state to its "1" condition. On the other hand, if the D input is logic-low before and during a clock pulse, the flip-flop changes state to its "0" condition. The D-type flip-flop is similar to a clocked R-S flip-flop, except that the input circuitry includes an inverter. Tests with logic pulsers and probes are made with respect to the truth table for the D-type flip-flop, as for any type of flip-flop. Therefore, it is essential for the digital technician to identify the kind of flip-flop with which he is concerned.

The JK master-slave flip-flop depicted in Fig. 4-10 is often encountered by the digital technician. Although it is more elaborate than the previously described flip-flops, the JK master-slave flip-flop has advantageous operating features. For example, a clock pulse will not cause any change of state if neither the J input nor the K input is enabled before the clock pulse is applied. If both the J input and the K input are enabled (logic high) before the clock pulse is applied, a change of state will occur upon application of the clock pulse. In case the output is logic-high before the clock pulse is applied, the output will be logic-low after the pulse arrives. On the other hand, in case the output is logic-low before the clock pulse is applied, the output will be logic-high after the pulse arrives. There are no indeterminate conditions.

Referring to Fig. 4-10A, the JK master-slave flip-flop is triggered by the trailing edge of the clock pulse. Note that the master section comprises the NAND gates A, B, C, and D. The slave section comprises the NAND gates E, F, G, and H, and the inverter I. Logic levels at the J and K inputs are transferred to the master flip-flop on the leading edge of a logic-high clock pulse and then stored until the trailing edge of the clock pulse arrives. At this time, the stored logic levels are transferred to the flip-flop. Note that in case the J input is enabled and the K input is disabled before a clock pulse arrives, the flip-flop will change state from "0" to its "1" condition. On the other hand, in case the K input is enabled and the J input is



(A) Configuration.

INITIAL CONDITIONS				FINAL CONDITIONS	
OUTPUTS		INPUTS		OUTPUTS	
1	0	J	K	1	0
LO	HI	LO	LO	LO	HI
LO	HI	LO	HI	LO	HI
LO	HI	HI	LO	HI	LO
LO	HI	HI	HI	HI	LO
HI	LO	LO	LO	HI	LO
HI	LO	LO	HI	LO	HI
HI	LO	HI	LO	HI	LO
HI	LO	HI	HI	LO	HI

(B) Truth table.

Fig. 4-10. A JK master-slave flip-flop.

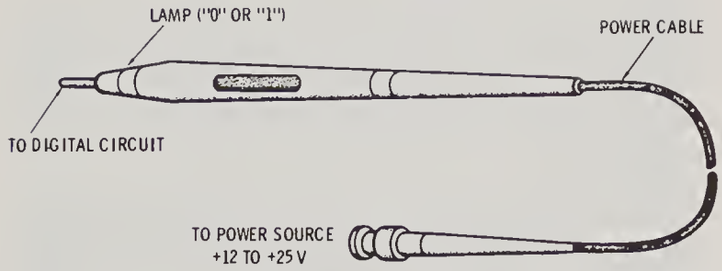


Fig. 4-11. High-level logic probe.

disabled before a clock pulse arrives, the flip-flop will change state from "1" to its "0" condition. Again, if neither the J input nor the K input is enabled before a clock pulse arrives, the flip-flop will remain in its initial state. Or, in case both the J input and the K input are enabled before a clock pulse arrives, the flip-flop will change state on the trailing edge of the logic-high clock pulse. These responses are summarized in the truth table in Fig. 4-10B.

HIGH-LEVEL LOGIC TESTING

High-threshold logic (HTL) can be tested with a high-level logic probe, illustrated in Fig. 4-11. This probe is similar to the logic probe described previously, except that it responds to higher input voltage levels and operates from power supplies in the 12- to 45-volt range. Its logic-high threshold is 9.5 volts, and its logic-low threshold is 2.5 volts. The probe will respond to pulse repetition rates of at least 5 MHz. A high-level logic probe can also be used to test metal-oxide semiconductor (MOS) logic, as explained subsequently. When the probe is applied at a logic-high terminal, a bright band of light appears around the probe tip. On the other hand, when it is applied at a logic-low terminal, the light goes out. Open circuits or voltages in the "bad-level" region between the preset thresholds cause lamp illumination at half brilliance. Single narrow pulses are stretched and will cause the lamp to flash on or blink off, depending on the pulse polarity.

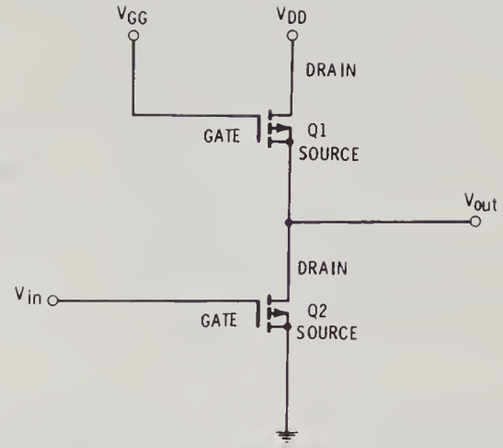


Fig. 4-13. Basic MOS inverter configuration.

EMITTER-COUPLED LOGIC PROBE

Emitter-coupled logic (ECL) can be tested with an ECL logic probe. As shown in Fig. 4-12, its logic-one threshold is −1.1 volts, and its logic-zero threshold is −1.5 volts. This is an example of positive logic, in which logic-one is a logic-high level and logic zero is a logic-low level. Note that in logic circuitry employing negative supply voltages, confusion may occur in determining functions. As an illustration, some manufacturers state that the more-negative voltage is *low* level and equal to a logical 1, and that the more-positive voltage is *high* level and equal to a logical 0. This more-positive voltage might be zero volts in some cases. Note that the majority of manufacturers adopt the following definition:

> *High* level is defined as the greatest voltage, whether positive or negative, from ground potential. *Low* level is the potential nearest ground, whether positive or negative.

An ECL probe is connected to a −5.2-volt power supply, either from the equipment under test or from an auxiliary power supply. It responds to pulse repetition rates up to 50 MHz (100 MHz at 50% duty cycle) and will indicate the presence of pulses with widths as small as 5 ns.

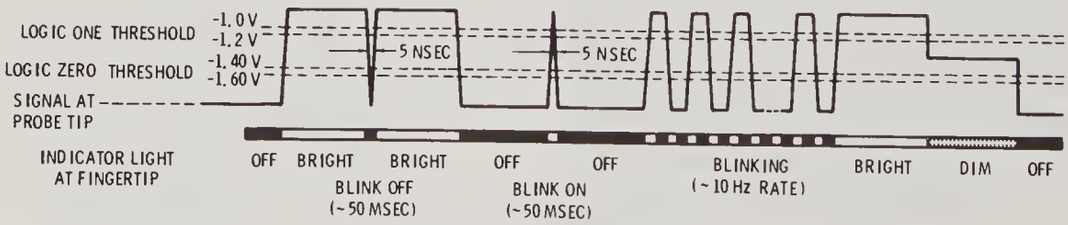
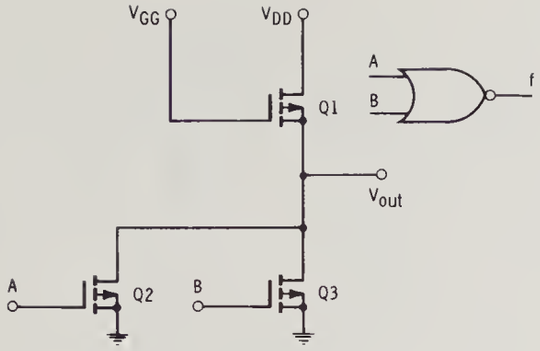


Fig. 4-12. Response of ECL probe to various input conditions.



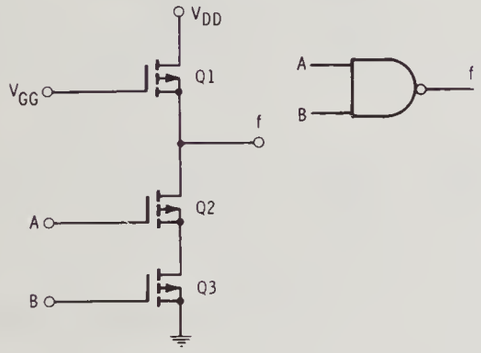
(A) Configuration.

(B) Truth table.

A	B	f
L	L	H
L	H	L
H	L	L
H	H	L

H = "1" ≅ V_{DD} = -12 V
L = "0" ≅ GND = 0 V

Fig. 4-14. A 2-input MOS NOR gate.



(A) Configuration.

(B) Truth table.

A	B	f
L	L	H
L	H	H
H	L	H
H	H	L

H = "1" ≅ V_{DD} = -12 V
L = "0" ≅ GND = 0 V

Fig. 4-15. A 2-input MOS NAND gate.

MOS LOGIC GATES

Metal-oxide semiconductor (MOS) digital ICs are used in the elaborate large-scale integrated circuits (LSI). Less-elaborate integrated circuits are called medium-scale integration (MSI). As noted above, MOS logic is in the high-threshold logic (HTL) family. MOS logic circuits have load resistors that are provided by metal-oxide semiconductor transistors (MOSFETS). Note that unlike other semiconductor logic designs, MOS logic

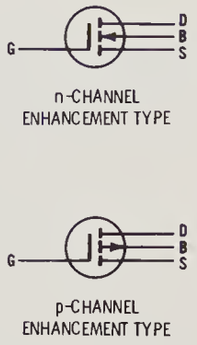


Fig. 4-16. Symbols for MOSFET transistors (G: gate, D: drain, B: bulk or substrate, S: source).

uses field-effect transistors instead of junction (bipolar) transistors. A basic MOS inverter arrangement is shown in Fig. 4-13. The device symbols indicate that Q1 and Q2 are p-channel enhancement-type FETs. In other words, they have characteristics that are similar to pentode vacuum tubes.

An MOS NOR gate is depicted in Fig. 4-14. Observe that this is an inverter configuration, with a third MOSFET, Q3, operating in parallel with Q2. This is a 2-input NOR gate. The logic-high level is −12 volts, and the logic-low level is approximately zero volts. Next, the basic inverter circuit can be elaborated to provide the NAND function, as shown in Fig. 4-15. A thrid MOSFET, Q3, is placed in series with Q2. These basic gates have low power dissipation and operate efficiently in low-speed logic applications. On the other hand, their high internal resistance (long time-constants) limits their response speed. Therefore, more-sophisticated MOS logic gates are used in high-speed logic applications. This topic is covered in greater detail subsequently.

COS/MOS LOGIC GATES

A subfamily of the MOS logic family is the complementary-symmetry/metal-oxide-semiconductor (COS/MOS) family. In this design, both p-channel and n-channel enhancement-type MOSFETS are integrated on the same chip. This design is inherently faster in response than MOS logic and provides a comparatively simple system design. Note that both p-channel and n-channel enhancement-type MOSFETs must be forward-biased in order to conduct. In other words, no useful channel conduction is obtained at zero bias or with reverse bias. Fig. 4-16 shows the schematic symbols for n-channel and p-channel enhancement-type MOSFETs. Circuits like the one shown in Fig. 4-17 are called complementary circuits. This circuit employs both p-channel and n-channel

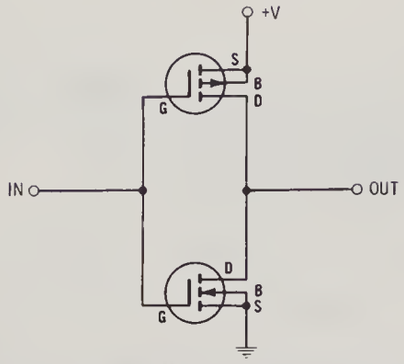


Fig. 4-17. A COS/MOS inverter circuit.

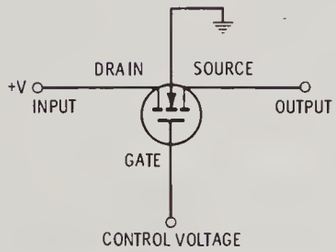


Fig. 4-18. A single n-channel MOSFET transmission gate.

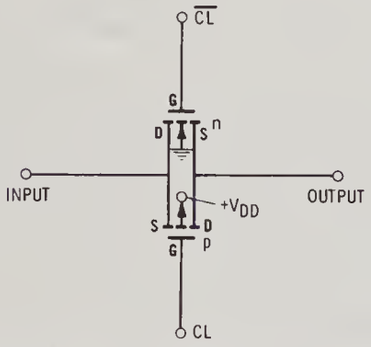


Fig. 4-19. COS/MOS transmission gate configuration.

MOSFETs in a complementary arrangement. Note that the drain terminals of the MOSFETs are connected together. This configuration provides a simple complementary inverter circuit.

Next, consider the single n-channel MOSFET transmission gate depicted in Fig. 4-18. This is essentially a single-pole single-throw (spst) switch. When the gate is driven positive, the transmission switch conducts. However, this simple switch is comparatively inefficient. Therefore, it is elaborated in practice, and a complementary-symmetry (COS/MOS) configuration is employed as seen in Fig. 4-19. Observe that a p-channel MOSFET is operated in parallel with an n-channel MOSFET. Simultaneous positive and negative clock pulses are utilized to drive the respective gates when the transmission gate is to be opened. However, a single control voltage suffices when

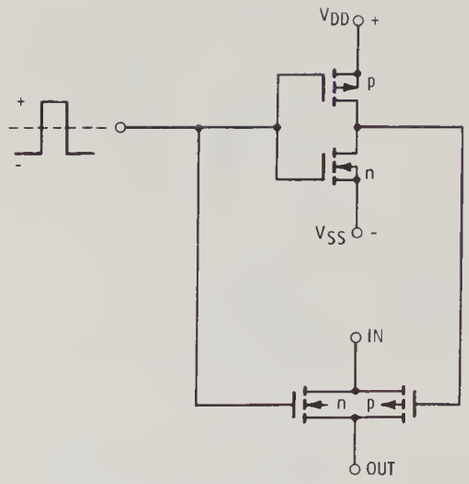


Fig. 4-20. Combination of COS/MOS transmission gate and inverter to form a switch.

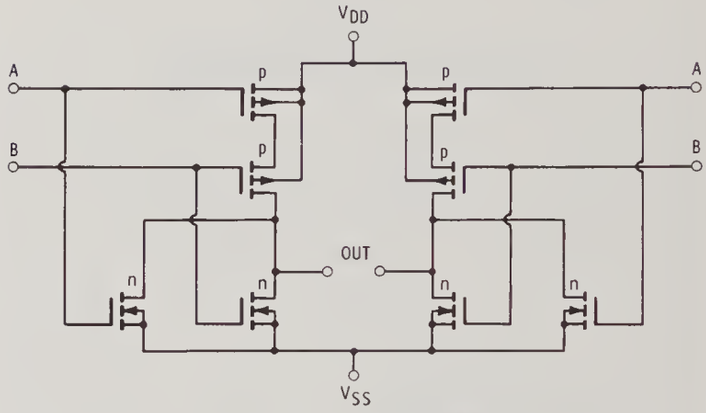


Fig. 4-21. A pair of 2-input COS/MOS NOR gates.

the transmission gate is combined with an inverter, as depicted in Fig. 4-20. In other words, the inverter is driven by a single control voltage and produces a pair of oppositely polarized output voltages for opening the transmission gate.

A 2-input COS/MOS NOR gate is shown in Fig. 4-21. (Actually, a pair of NOR gates appears in the diagram.) This type of NOR gate comprises an inverter with two n-channel MOSFETs in parallel and two p-channel MOSFETs in series. Each of the two inputs is connected to the gate of one n-channel and one p-channel MOSFET. A negative output is obtained when either the A or the B input is positive because the positive input will turn off its associated p-channel MOSFET and the output is thus disconnected from the V_{DD} supply. The associated n-channel MOSFET is turned on at the same time, which effectively connects its drain to ground and provides a low output. When both input signals are zero (ground potential), both p-channel MOSFETs turn on and

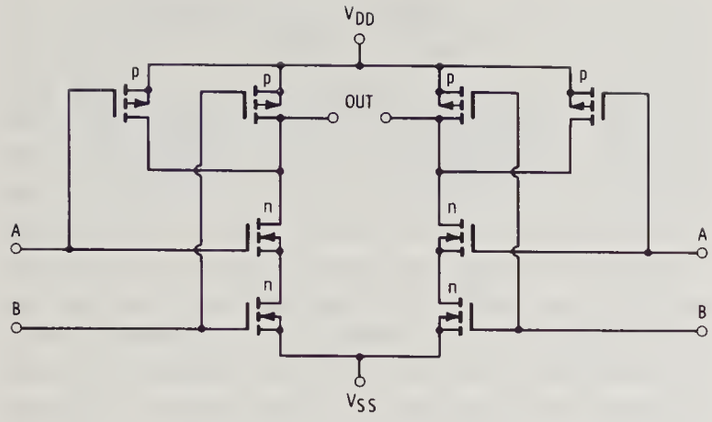


Fig. 4-22. A pair of COS/MOS NAND gates.

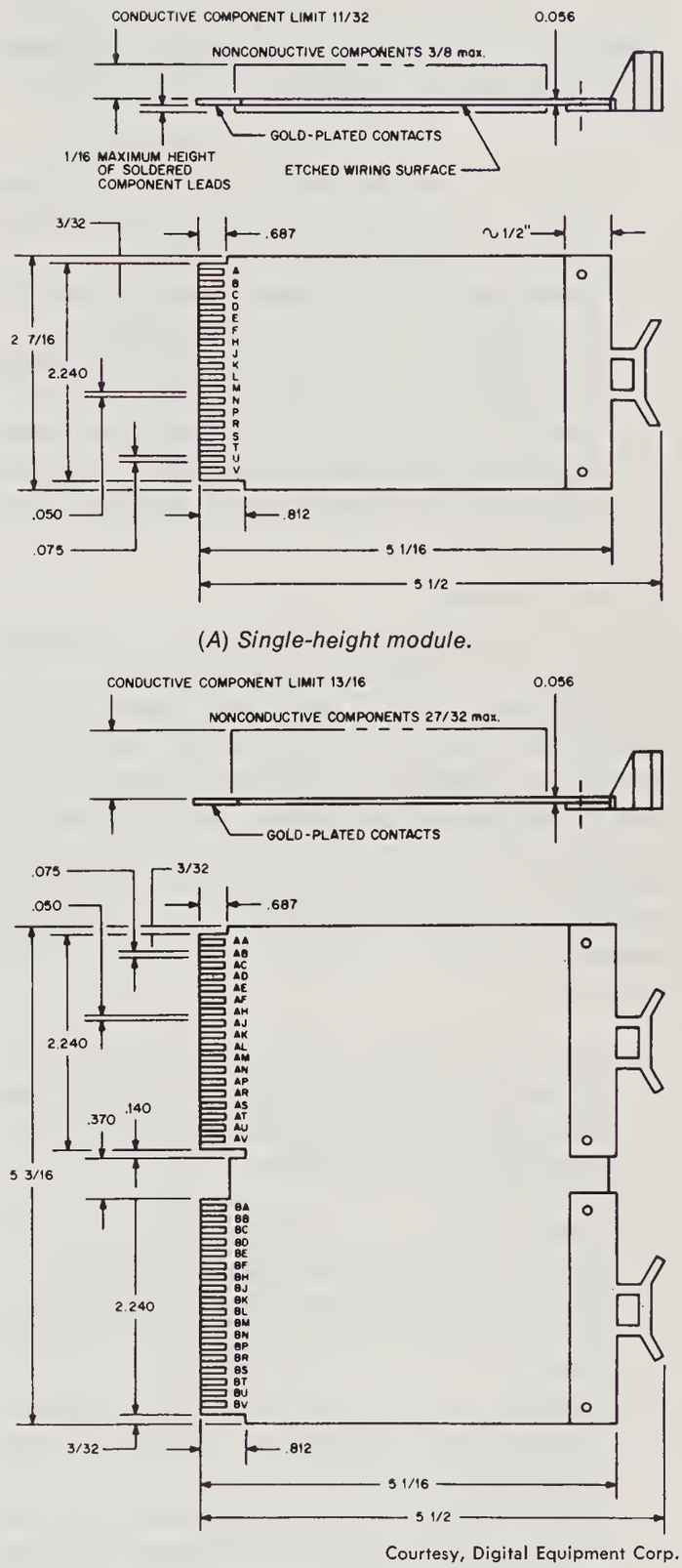
both n-channel MOSFETs turn off. In turn, the output is connected to the V_{DD} supply voltage, and a high output occurs. Note that an OR gate can be formed by adding an inverter to the output of the NOR gate.

Next, Fig. 4-22 depicts a COS/MOS NAND gate. It comprises an inverter with two n-channel MOSFETs in parallel and two n-channels MOSFETs in series. Note that the output will go negative only when both inputs are positive, in which case the p-channel MOSFETs are turned off and the n-channel MOSFETs are turned on. Thus, the output is connected to ground. On the other hand, if either of the inputs is negative, its associated n-channel MOSFET is turned off and its associated p-channel MOSFET is turned on. Thus, the output is connected to the V_{DD} supply voltage, and the output is high. Note that an AND gate can be formed by adding an inverter to the output of a NAND gate. Power-supply voltages for COS/MOS digital devices from 1.5 to 16 volts, 10 volts being nominal.

TROUBLESHOOTING TECHNIQUES

1. "Stuck-At" Condition

When a digital system or subsystem does not respond to input pulses, and the output maintains some arbitrary indication, the condition is called a "stuck-at" trouble symptom. Preliminary analysis is usually made by evaluating the block diagram for the digital system and then by making pulse-tracing tests with a logic probe or logic clip. If the fault is localized to a plug-in module, the module can then be replaced with a known-good module to see if normal operation resumes. This procedure minimizes downtime, and the defective module can either be repaired at some future time or perhaps discarded. On the other hand, if the digital system does not utilize modular construction, the faulty component must be lo-



(A) *Single-height module.*

(B) *Double-height module.*

Courtesy, Digital Equipment Corp.

Fig. 4-23. Physical features of typical modules.

cated and replaced. Fig. 4-23 shows the physical features of typical modules used in logic systems. Common causes for "stuck-at" trouble symptoms are:

a. Open or shorted circuit-board conductor, such as the output-X conductor in Fig. 4-1.
b. Subnormal power-supply voltage.
c. Defective IC that seriously distorts the digital waveform (check with oscilloscope).
d. Accidental replacement of a defective IC with an "equivalent" IC from another logic family.
e. Clock drifting to excessively high frequency (measure repetition rate with triggered-sweep scope). Replace clock section, if required.

2. Pulse Dropouts

A pulse that has less than threshold amplitude will effectively "drop out" and will have no more triggering action than a completely missing pulse. Accordingly, when a digital system has either erratic or consistently incorrect response, the pulse trains should be checked both for missing pulses and for pulses that might have subnormal amplitudes. As noted previously, each type of digital logic has its specified pulse amplitudes. Common causes for pulse dropout trouble symptoms are:

a. Leakage between circuit-board conductors. Inspect circuit board for dirt, dust, grime, and grease. Clean with solvent and brush. If corrosion has accumulated, replace the circuit board.
b. Poor contacts in module receptacle. Check incoming and outgoing pulses with scope.
c. Marginal IC in pulse channel. Make pulse-tracing tests with a scope or logic pulser and probe.
d. Defective or poor power-supply regulation. Monitor with voltmeter to confirm or clear suspicion.
e. Faulty indicator unit, giving same symptom as logic trouble. Check input pulses to indicator unit with scope.

3. Aliasing or Introduction of Spurious Pulses

Aliasing symptoms may be random or consistent in occurrence. In either case, aliasing can sometimes be localized to a particular sub-system by analyzing the symptom with respect to the block diagram for the complete digital system. As an illustration, if the "4" indicator in a binary counter triggers twice each time that its flip-flop is pulsed, the technician would conclude that the flip-flop is defective or that the applied trigger waveform is abnormal. On the other hand, the occurrence of spurious pulses may be distributed so widely throughout a digital system that systematic tests are required to narrow down the trouble possibilities. In such situations, a properly operating subsystem can generally be eliminated from suspicion by monitoring it with scopes. Common causes of aliasing or introduction of spurious pulses are:

a. Abnormally high noise fields surrounding the digital installation. Check for sparking electrical machinery, defective power wiring, or unusual power switching operations.
b. Glitches fed into digital system from defective power supply. Check with scope. Repair or replace power supply as required.
c. Defective neon sign(s) operating in the vicinity.
d. Strokes of lightning in the vicinity.
e. IC malfunction. Make pulse-tracing tests with a scope or logic pulser and probe.

4. Intermittent Operation

Intermittent operation of gates and associated digital circuits is commonly caused by the faults and abnormal conditions that have been previously noted. However, in case intermittent operation cannot be tracked down to defective contacts, device malfunction, or component defects in the digital system, remember that the trouble may be located in the readout system. For example, an indicator lamp sometimes becomes intermittent; in a case history, the solder joint at the base of a lamp was defective. Since connectors are common troublemakers, the following possible faults should be kept in mind:

a. Check recessed pins; if a pin has slipped back into the connector body, an intermittent condition can result. A retaining clip may be broken or missing, or a plastic recess catch might be broken.
b. Look for loose-fitting connector pins. For example, a pin might have been pushed to one side, instead of mating properly.

c. Check for cracked or broken plastic connectors.
d. Inspect the clamp that secures the wire leads entering the back of the connector. A bare-wire contact with a metal clamp is likely to produce intermittent operation.
e. Make certain that the threads on threaded metal connectors are not defective and that guide pins are not missing.

CHAPTER 5

Display Devices and Operation

Various types of display devices are used for readout of counters. Incandescent lamps operating in transistor emitter circuits were discussed previously. Other types of lamps are also employed, such as Nixie® tubes, Numitrons, Panaplex plates, light-emitting diodes (LEDs), liquid-crystal displays, and electrofluorescent tubes. Alternatively, digital equipment may utilize punched-tape, punched-card, or automatic typewriter readout. Older designs provided arrays of conventional neon bulbs for readout. Some display devices operate at low voltages, while others operate at comparatively high voltages. Current requirements also vary. Sophisticated display devices may optimize operating efficiency by means of time-sharing or multiplexing circuitry. Accordingly, the digital technician may encounter complex decoder/driver circuitry between counters and display devices.

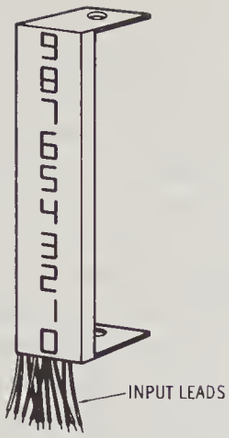
Common trouble symptoms caused by faults in display devices and their associated circuitry are:

1. Display device on continuously, or off continuously.
2. Incorrect readout displayed.
3. Failure to start counting from zero.
4. Intermittent operation.

GENERAL DISCUSSION

Older digital-equipment designs that employ arrays of conventional neon bulbs for readout have translucent screens such as shown in Fig. 5-1. This type of display is comparatively difficult to read because the numerals are not lined up horizontally. Digital equipment of somewhat more recent design employs a specialized form of neon lamp called a Nixie tube. It consists of a "stacked" series of ten wire cathodes, each having the shape of a numeral and contained in a single neon lamp. A Nixie-tube display appears in Fig. 5-2. Obviously, it is much easier to read than a simple neon-bulb array. Another type of display tube, called the Numitron, is illustrated in Fig. 5-3. It is a vacuum tube that contains seven separate wire filaments (segments) mounted on an insulating plate. Various combinations of segments are energized to display different numerals.

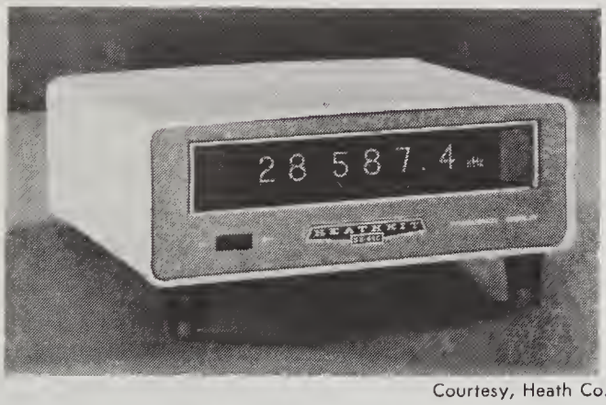
Another type of display tube, shown in Fig. 5-4, employs a segmental arrangement of cold-cathode electrodes. It operates on the same principle as the neon bulb and has a threshold voltage of 180 volts. Recently designed display devices often employ light-emitting diodes (LEDs). Typical LEDs and operating characteristics are depicted in Fig. 5-5. An LED consumes very little power and operates on either ac or dc at approximately 2 volts. However, they are quickly damaged by overheating, and a heat sink or equivalent must be used during soldering procedures. The effective resistance of an LED is approximately 39 ohms. Seven-segment display devices comprising two LEDs per segment are used in some digital equipment, as depicted in Fig. 5-6. Another typical dis-



(A) Columnar display of neon bulbs.

(B) Readout of number 175, 296.

Fig. 5-1. Neon-bulb and translucent-screen display.



Courtesy, Heath Co.

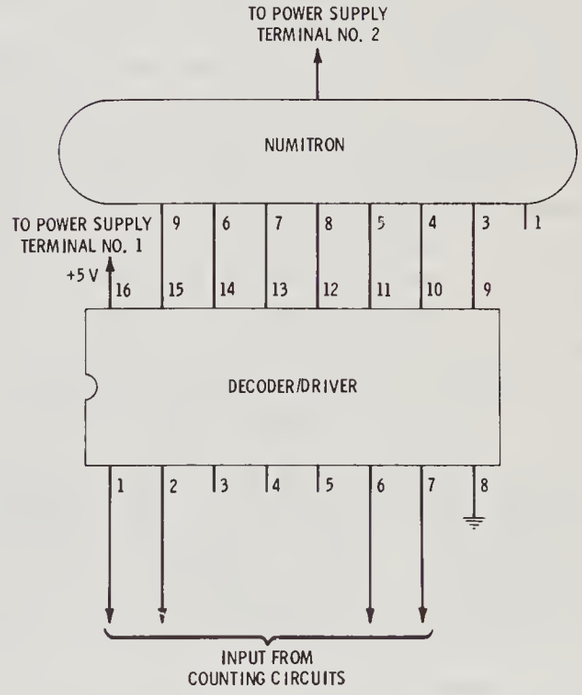
Fig. 5-2. Example of a Nixie®-tube display.

play arrangement of LEDs is shown in Fig. 5-7. Note that LEDs may be connected in either common-cathode or common-anode configurations, depending on the polarity of the supply voltage.

Liquid-crystal displays are used in some of the more recent types of digital equipment. This type of display device uses an organic substance that is ordinarily transparent. However, when subjected to an electrostatic field, the liquid tends to crystallize and becomes opaque. Fig. 5-8 shows the layout of a segmented liquid-crystal display. This

(A) Appearance.

(B) Arrangement of filament segments.



(C) Block diagrams of driver system.

Fig. 5-3. The RCA Numitron display tube.

Fig. 5-4. A segmental cold-cathode display tube.

type of readout consumes very little power but requires at least 25 volts. Another version of this device, called the field-effect liquid-crystal display, makes use of an organic substance that changes the light polarization in response to an electrostatic field. The readout assembly includes a pair of transparent polarizing sheets. An advantage of the field-effect liquid-crystal display device is that it operates at comparatively low voltage.

Electrofluorescent display tubes are also used in some digital equipment. This display device has much the same external appearance as the segmental cold-cathode display tube shown in Fig. 5-4. However, an electrofluorescent display tube is functionally related to the cathode-ray tube. In other words, it comprises one or two heater wires mounted in front of a phosphor-coated, seven-segment pattern. The heater wires emit electrons, which are attracted to the phosphor-coated segments. An accelerating voltage of 25 or 30 volts is required to produce a glow from a segment. The filament voltage is typically 1 volt. Although the efficiency of an electrofluorescent display is comparatively low, display multiplexing can be utilized to increase the operating efficiency. This topic is detailed subsequently.

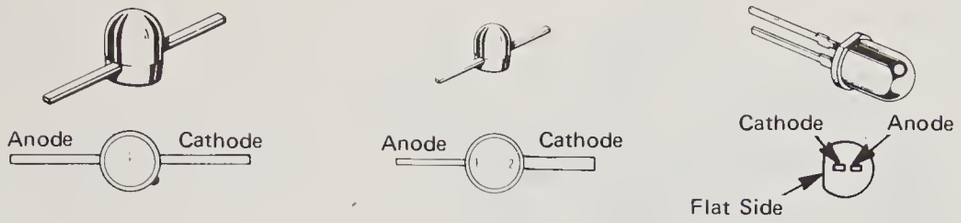
DECODER/DRIVER ARRANGEMENTS

Decoder/drivers are used to switch the various elements in a display device off or on in order to display the numbers that correspond to the states in a counter chain. The first section of the arrangement consists of a flip-flop chain with four outputs, A-B-C-D, as depicted in Fig. 5-9. In other words, A is the output of FF4, B is the output of FF3, and so on. Referring to Fig. 5-9B, it is helpful to think of the ABCD output as a binary number, since it consists of 0's and 1's. This binary counter counts up to 15 and then automatically resets to zero on the 16th trigger. Therefore, the next section of the decoder/driver arrangement consists of a modification of the basic binary counter so that after reaching a count of 9, it will automatically reset on the 10th trigger. Various methods are used to perform this function in digital-equipment designs.

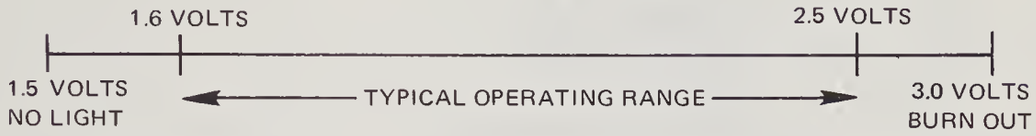
A common method of obtaining a 9 count followed by reset is shown in Fig. 5-10. Observe that output A from flip-flop FF4 is fed to a NOT circuit, which in turn feeds the inputs of FF2 and FF3. This NOT circuit has no effect on counter operation until FF4 is triggered by FF3. Note that FF4 will be triggered on the 8th count. In case the NOT circuit were disconnected, the binary counter would read out 1000 on the 8th count. On the other hand, at the instant that FF4 changes state, its output changes from 0 to 1; this 1 drives the NOT circuit, which in turn applies a 0 output to FF2 and FF3. Therefore, flip-flops FF2 and FF3 change state and the ABCD readout is 1110 on the 8th count. Next, on the 9th count, D has a 1 readout, so the ABCD readout is 1111. Finally, on the 10th count, reset occurs in the usual manner, and the ABCD readout is 0000. Since the NOT circuit goes to a 1 output, there is no response from FF2 and FF3 on reset.

To summarize briefly, the preceding modification of the basic binary counter corresponds to the decimal-counter truth table shown in Fig. 5-11. The next section in the decoder/driver arrangement employs logic gates to convert the ABCD values of Fig. 5-11 to 10 sequential pulses for actuating 10 display devices (0 to 9). Thus, the main block diagram for the decoder/driver appears as shown in Fig. 5-12. This is often called a 4-10 decoder. The logic gates are arranged as depicted in Fig. 5-13. Referring to Fig. 5-12, observe that each of the outputs A, B, C, and D is fed to various logic configurations. Thus, as seen in Fig. 5-13, the first logic configuration comprises four inverters and an AND gate which drives the 0 display device, while the second logic configuration comprises three inverters and an AND gate which drives the 1 display device. Again, the third

(*A*) *Case styles.*



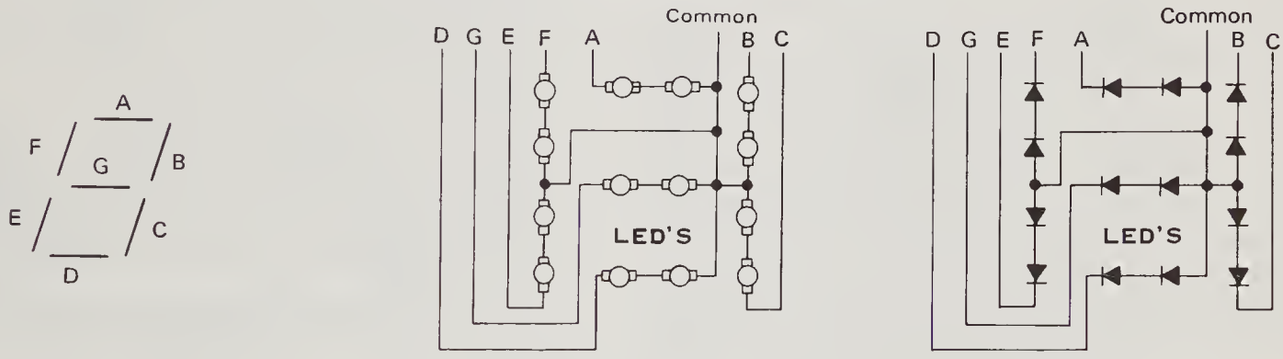
(*B*) *Operating characteristics.*



HEP Type No.	Reverse Voltage V_R (Volts)	Forward Current I_F (mA)	Power Dissipation P_D (mW)	Brightness f_L (Typical)
P2000	4.0	50	100	450
P2001	3.0	40	120	750
P2003	4.0	50	100	50
P2004	4.0	20	120	750
P2005	4.0	60	100	–

Courtesy, Motorola Inc.

Fig. 5-5. Typical light-emitting diodes.



(*A*) *Segment arrangement.* (*B*) *Layout of two LEDs per segment.* (*C*) *Schematic diagram.*

Fig. 5-6. A seven-segment display arrangement that uses two LEDs per segment.

Fig. 5-7. Another LED display arrangement.

logic configuration comprises three inverters and an AND gate, while the fourth logic configuration comprises two inverters and an AND gate. A total of ten logic configurations are employed in the binary-to-decimal converter of the decoder/driver.

Note in Fig. 5-13 that all of the logic configurations have paralleled inputs. In other words, the A, B, C, and D counter outputs are applied simultaneously to all of the gates. However, only one of the gates can respond at any one time and actuate a display device. The reason for this is that any one of the AND gates must have four "1" inputs

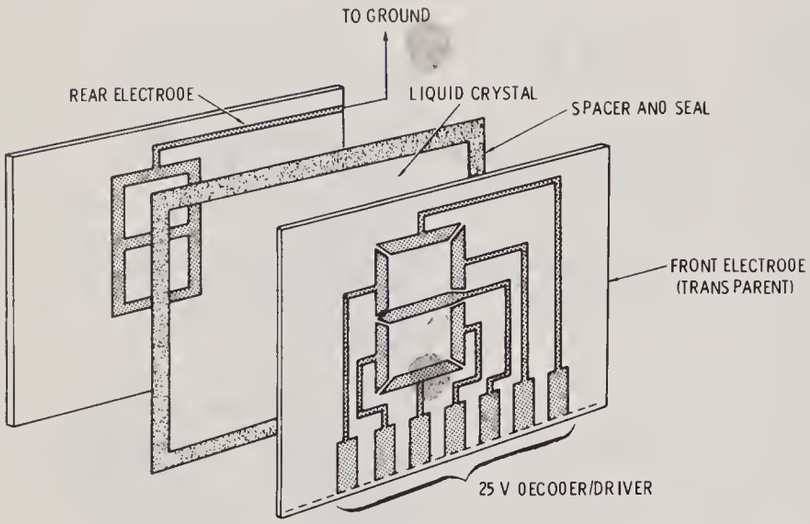
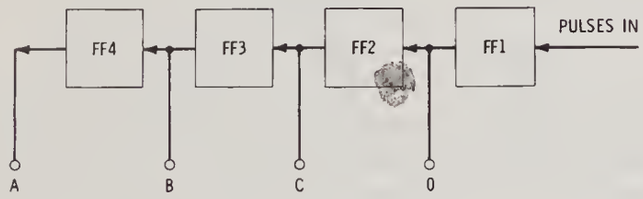


Fig. 5-8. Layout of a liquid-crystal display device.



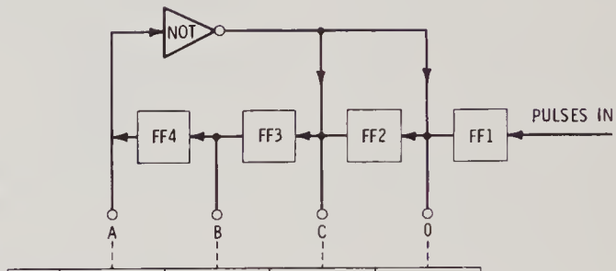
(A) Block diagram.

NUMBER OF TRIGGERS	A	B	C	D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1
16	0	0	0	0

(B) Truth Table.

Fig. 5-9. Binary counter with four outputs.

simultaneously before it will produce a "1" output level and actuate its display device. Observe that each of the gates has its particular combination of inverter and direct inputs. Therefore, a particular combination of "1" and "0" inputs is required from the counter to actuate a given gate. These individual combinations of "1's" and "0's" are set forth in Fig. 5-11, which shows the truth table for



0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
(8)	(1)	(0)	(0)	(0)	FORBIDDEN RESPONSE
8	1	1	1	0	MODIFIED BINARY CODE
9	1	1	1	1	
10	0	0	0	0	RESET

Fig. 5-10. A nine count followed by reset, due to the NOT circuit.

	A	B	C	D
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	1	1	0
9	1	1	1	1
10	0	0	0	0

Fig. 5-11. Decimal-counter truth table.

the modified basic binary counter. As another example of the logic circuitry in the binary-to-decimal converter, Fig. 5-14 shows the logic circuit for the 8 display device.

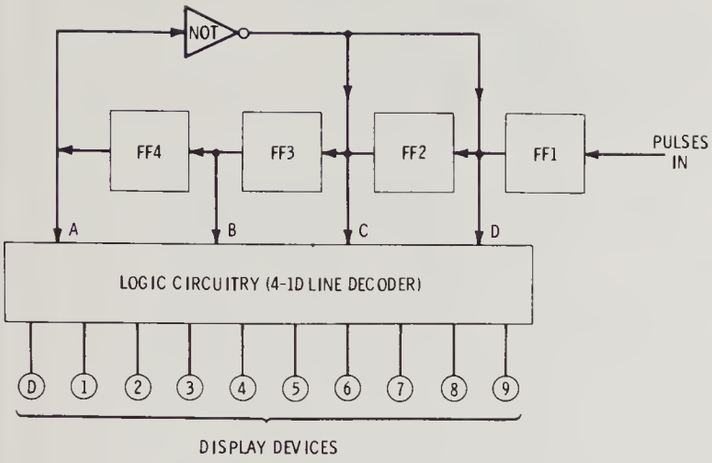


Fig. 5-12. Main block diagram for decoder/driver.

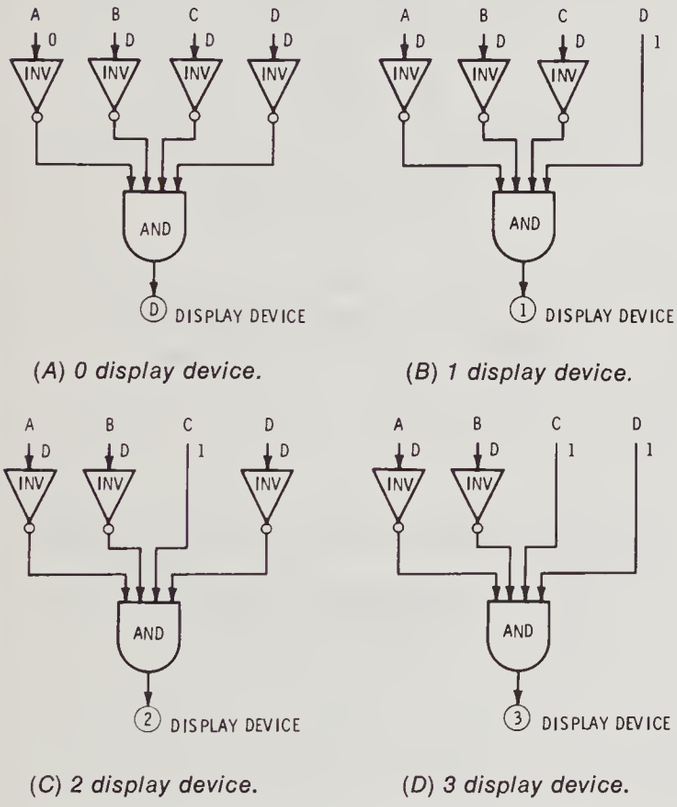


Fig. 5-13. First four logic circuits for the binary-to-decimal converter.

Next, it will be recognized that the logic circuits can be simplified, and the inverter gates indicated in Fig. 5-13 can be eliminated. Since a flip-flop has both an uninverted and an inverted output, its inverted output can be employed instead of feeding its uninverted output through an inverter. Thus, FF4 in Fig. 5-12 has both $\underline{A}$ and $\overline{A}$ outputs available; FF3 has both B and $\overline{B}$ outputs available; FF2 has both C and $\overline{C}$ outputs available; and FF1 has both D and $\overline{D}$ outputs available.

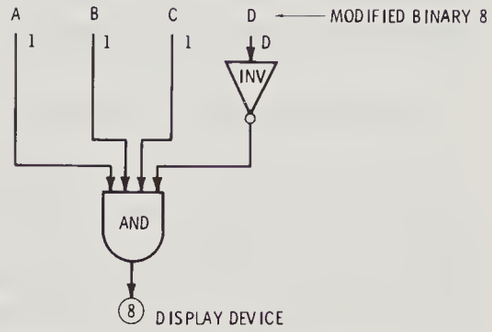


Fig. 5-14. Logic circuit for the 8 display device.

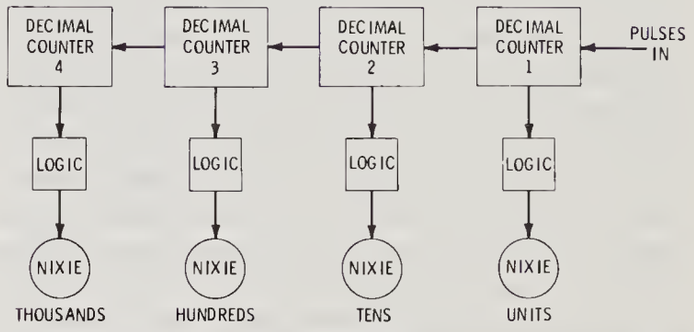


Fig. 5-15. Counter arrangement with a decimal readout capacity of 9999.

Therefore, with reference to Fig. 5-13A, it is feasible to drive the AND gate with the $\overline{A}$, $\overline{B}$, $\overline{C}$, and $\overline{D}$ outputs from the counter and to dispense with the inverters. Similarly, it is feasible to drive the AND gate in Fig. 5-13B with the $\overline{A}$, $\overline{B}$, and $\overline{C}$ outputs from the counter, but keeping the D output from the counter and thereby dispense with the inverters. Again, it is feasible to drive the AND gate in Fig. 5-14 with the $\overline{D}$ output from the counter, but keeping the A, B, and C outputs and thereby dispense with the inverter.

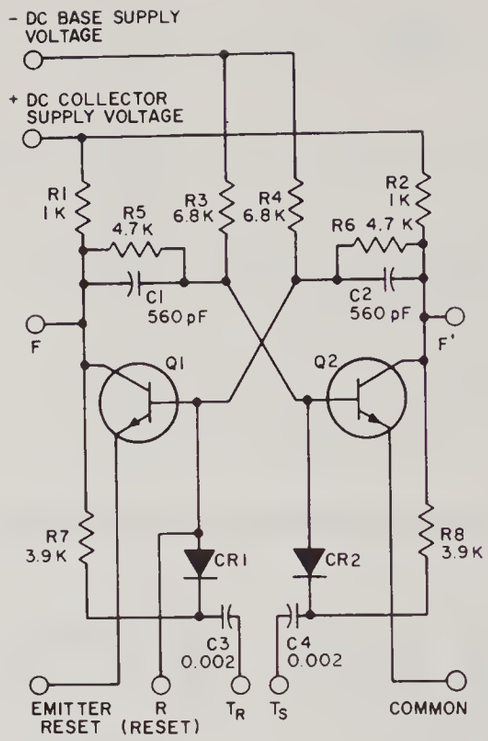
These decoder/driver arrangements provide direct decimal readout of numbers from 0 to 9. To increase the capacity of this basic counter, additional counters (with decoder/drivers) are connected in cascade, as shown in Fig. 5-15. On the 10th trigger, the units counter resets to its zero state and couples a negative trigger into the tens counter, which in turn advances one count. Next, after the tens counter has processed ten triggers, it resets to its zero state and causes the hundreds counter to advance one count. Again, after the hundreds counter has processed ten triggers, the thousands counter advances one count. On the 10,000th input trigger, the entire system resets to its zero state. If more capacity is required in a

particular unit of digital equipment, additional counters are added to the system.

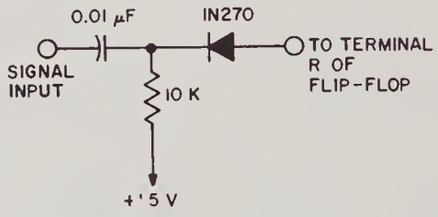
COUNT-BY-TEN COUNTING CIRCUIT

Another counter circuit used in various types of digital equipment is the count-by-ten, or decade, counting circuit shown in Fig. 5-16. A discrete-component circuit diagram and functional description of the counter are instructive at this point. Fig. 5-17 shows the circuit diagram for the flip-flop used in this counter circuit. As in the case of a simple binary counter, the counting process can start at any point in the counting cycle. However, we will stipulate that the count is to begin at zero, with each flip-flop set at zero, so that the F′ outputs in Figs. 5-16 and 5-17 are low (zero). Note that this zero set can be accomplished by pulsing the R (reset) terminal, or the emitter reset terminal. This discussion assumes that manual emitter reset is utilized with a push-button switch that momentarily opens the emitter circuit. If the R (reset) terminal is used to reset the flip-flop to its zero state, the circuit shown in Fig. 5-17B is employed. Note that reset details have been omitted from the block diagram in Fig. 5-16, as these are arbitrary.

It is helpful to briefly note the basic operation of the flip-flop depicted in Fig. 5-17A. The mode of operation that is obtained depends on how the input terminals T_R and T_S are connected. Referring to Fig. 5-16, observe that T_R and T_S are tied together in flip-flops "1," "2," and "4." This configuration is called a *toggle* flip-flop. Next, note that T_R and T_S are connected to different signal sources in flip-flop "8." This configuration is called a *set-*



(A) Flip-flop configuration.



Courtesy, RCA

(B) Circuit for resetting through the R (reset) terminal.

Fig. 5-17. Circuit diagram of the flip-flop in the decade counter.

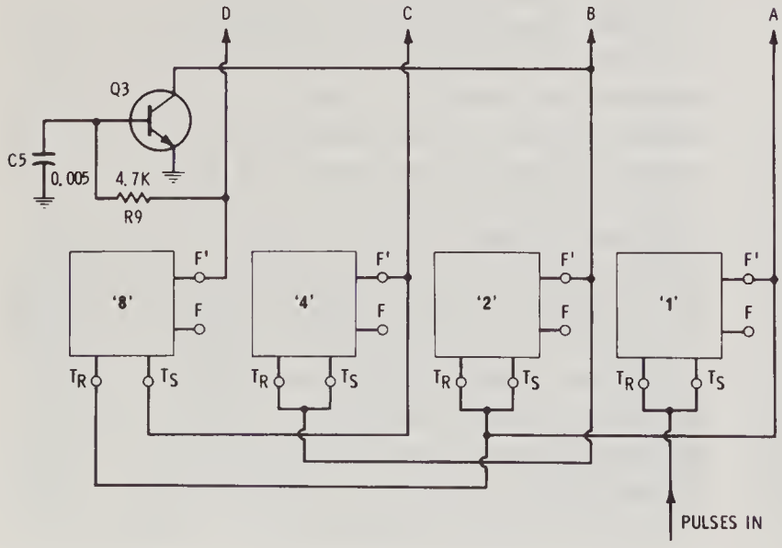


Fig. 5-16. Block diagram of a count-by-ten (or decade) counting circuit.

reset flip-flop. A toggle flip-flop is so-called because it changes state analogously to a toggle switch each time that a trigger pulse is applied. As noted previously, diodes CR1 and CR2 block positive pulses; only negative pulses can reach the bases of the transistors to turn off the one that is conducting and change the state of the flip-flop.

Note that a flip-flop cannot change its state unless a trigger pulse is applied or unless the emitter current of the conducting transistor is interrupted. In other words, the bias applied to one transistor by the other locks both transistors in their prevailing state. A transistor that is turned off is often said to "go high," and a transistor that is turned on is said to "go low." Note also that the condition at the output terminals associated with each transistor follows the same terminology. That is, when transistor Q1 is low, output terminal F is said to be low also. Again, when a transistor is set high, its output logic level is said to be a binary 1, and when a transistor is set low, its output logic level is said to be a binary 0.

Observe next that when a transistor changes state from low to high, or from 0 to 1, a positive logic level is produced at its output terminal. On the other hand, when the transistor goes from high to low, or from 1 to 0, a negative logic level is produced at its output terminal. This negative-going logic level is used to trigger the succeeding flip-flop in the decade counter shown in Fig. 5-16. Note that when the T_R and T_S terminals are not connected together, but are energized from different sources, more than one kind of response can be obtained. For example, suppose that transistor Q2 is turned on and that a negative pulse is applied to T_S in Fig. 5-17, thereby turning Q2 off and setting output terminal F′ high (1). Then, as Q2 turns off, it turns Q1 on and changes the state of the flip-flop.

On the other hand, suppose that Q2 in Fig. 5-17 is already off, which means that output F′ is at the logic-high level. Then, the negative pulse will have no effect on Q2 and will not change the state of the flip-flop. Consider, however, the result of applying a negative pulse to T_R in this situation. It is apparent that Q1 will be turned off, which will turn Q2 on, and output terminal F′ will go logic-low. However, if Q2 were on and output F′ were already logic-low, a negative pulse applied to T_R would have no effect and the flip-flop would remain in its prevailing state. To summarize briefly, the chief difference between a toggle flip-flop and a set-reset flip-flop is that the toggle flip-flop always changes state when a negative trigger pulse is applied. On the other hand, the set-reset flip-flop will change state only when that conducting transistor is driven by a negative trigger pulse.

Note in passing that more than one input signal path to the flip-flop transistors in Fig. 5-17 may be utilized. The R (reset) terminal is driven when it is desired to know that transistor Q1 is nonconducting. In other words, a negative pulse applied to terminal R turns Q1 off in case it is on, which changes output F from logic-low to logic-high and changes the state of the flip-flop. However, if Q1 happens to be off already, the negative pulse will produce no response. Next, observe that if a positive trigger pulse is applied at the emitter-reset terminal (or if the emitter circuit is momentarily opened, the flip-flop will reset to the state represented by zero in the counter—output F high (1) and output F′ low (0).

Now, observe the truth table for the count-by-ten, or decade, counting circuit, shown in Fig. 5-18. It is evident that each decimal count is represented by its actual corresponding binary number. Thus, this counter operates differently from the counter depicted in Fig. 5-10. When the first negative pulse is applied at the pulse-input terminal in Fig. 5-16, the "1" flip-flop changes state from 0 to 1, and an indicator lamp connected to the A output will glow. On the next negative input pulse, the "1" flip-flop changes state back to 0 and applies a negative pulse to the "2" flip-flop, which in turn changes state from 0 to 1. Accordingly, the A-output lamp extinguishes, and the B-output lamp glows, indicating a count of 2 in binary readout. On the third negative input pulse, the "1" flip-flop changes state from 0 to 1, causing the A-output lamp to glow again. Since the change of state from 0 to 1 does not produce a negative pulse to change the state of the "2" flip-flop, the B-output lamp continues to glow, and a count of 3 is indicated in binary readout.

As successive negative pulses are applied to the pulse-input terminal in Fig. 5-16, the flip-flops change state progressively as noted in the truth table of Fig. 5-18. For example, application of a 7th-input pulse causes the A-, B-, and C-output lamps to glow for a count of 7 in binary readout. Next, observe that the inputs to the "8" flip-flop

are connected in a so-called split-toggle configuration. This means that once a transistor in the "8" flip-flop is turned off, it will remain off and at the same time will hold the other transistor on until such time that the conducting transistor receives a negative pulse to turn it off. Thus, on the 8-input pulse, the F′ output of the "8" flip-flop is set to logic-high by the negative (logic-low) pulse input to terminal T_S of the "8" flip-flop from the "4" flip-flop while the latter changes state from logic-high to logic-low. The negative pulses fed to input T_R of the "8" flip-flop from the "1" flip-flop have no effect, since the transistor connected to terminal T_R is already off and cannot be triggered by negative pulses.

Observe also that when the count proceeds from 7 to 8, and the D-output lamp glows while all the other lamps extinguish, a logic-low pulse is fed via transistor Q3 to the "2" flip-flop. This pulse is applied at the F′ output (Fig. 5-16) and clamps the "2" flip-flop in its logic-low state. In other words, Q3 in Fig. 5-16 inverts the logic-high level of the D output and clamps the F′ output of the "2" flip-flop virtually at ground potential. Next, when the 9th input pulse is applied, the "1" flip-flop changes state and the A-output lamp glows for a count of 9 in binary readout. Finally, the 10th input pulse causes the "1" flip-flop to change state from logic-high to logic-low, thereby feeding negative trigger pulses to the "2" flip-flop and to the T_R terminal of the "8" flip-flop. Accordingly, the "8" flip-flop changes state to logic-low, but the "2" flip-flop is unable to change its state because of the clamping action of transistor Q3. All of the indicator lamps are now extinguished and the counter has been reset. Observe that the "2" flip-flop would have changed its state during reset except for the fact that C5 holds the forward bias on the base of Q3 until after the 10th pulse has passed.

Only one decade counter is shown in Fig. 5-16. However, if another counter is connected into the chain (see Fig. 5-15), the second counter will indicate 1 when the first counter resets. In other words, when the D-output line in Fig. 5-16 goes from logic-high to logic-low, it produces a negative pulse that can be used to trigger the first flip-flop in the second counter. As a result, a count of 10 will be indicated instead of a zero count. Observe that this count of 10 will be a binary readout. If a decimal readout is desired (as is usually the case), A-, B-, C-, and D-output lines from the counter(s) must be connected to suitable gating circuits for operation of lamps or other decimal display devices. These gating circuits are arranged in accordance with the truth table shown in Fig. 5-18, as explained for the earlier example.

COUNT	"8"	"4"	"2"	"1"	(SECOND COUNTING CIRCUIT) "1"
0	0	0	0	0	
1	0	0	0	1	
2	0	0	1	0	
3	0	0	1	1	
4	0	1	0	0	
5	0	1	0	1	
6	0	1	1	0	
7	0	1	1	1	
8	1	0	0	0	
9	1	0	0	1	
10	0	0	0	0	1

Fig. 5-18. Truth table for the decade counting circuit in Fig. 5-16.

It is instructive to note the circuit-board layout for the decade (count-by-ten) counter shown in Fig. 5-19. When troubleshooting a counter configuration, it is necessary to correlate the block diagram with the circuit diagram, which in turn must be correlated with the circuit-board layout. With each component identified on the circuit-board layout, it is a comparatively easy procedure to go from a particular block or point in Fig. 5-16 to one or more of the associated components in Fig. 5-17, and thence to the corresponding location(s) on the circuit board in Fig. 5-19. An important caution to keep in mind when working with discrete-component boards is to observe correct polarity when replacing diodes. For example, with reference to Fig. 5-17, the specified diode polarities must be maintained. Accidental reversal of a replacement diode will result in new trouble symptoms that can be quite baffling to the apprentice technician.

TROUBLESHOOTING TECHNIQUES

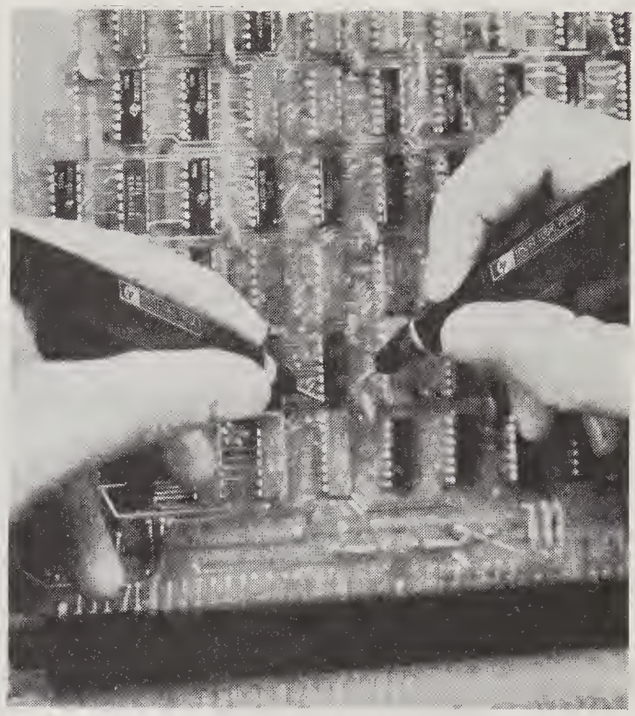
1. Display Device On Continuously, or Off Continuously

This trouble symptom can take various forms. In a typical situation, Nixie® tubes are used as display devices and all the tubes glow continuously with a zero readout. Since the Nixie tubes are glowing, the technician knows that they are receiving power. In turn, the most likely fault is a lack of input pulses to the units counter. An oscilloscope check should be made. Note, however,

that other malfunctions can cause the same trouble symptom. Common causes for Nixie tubes glowing continuously with a zero readout are:

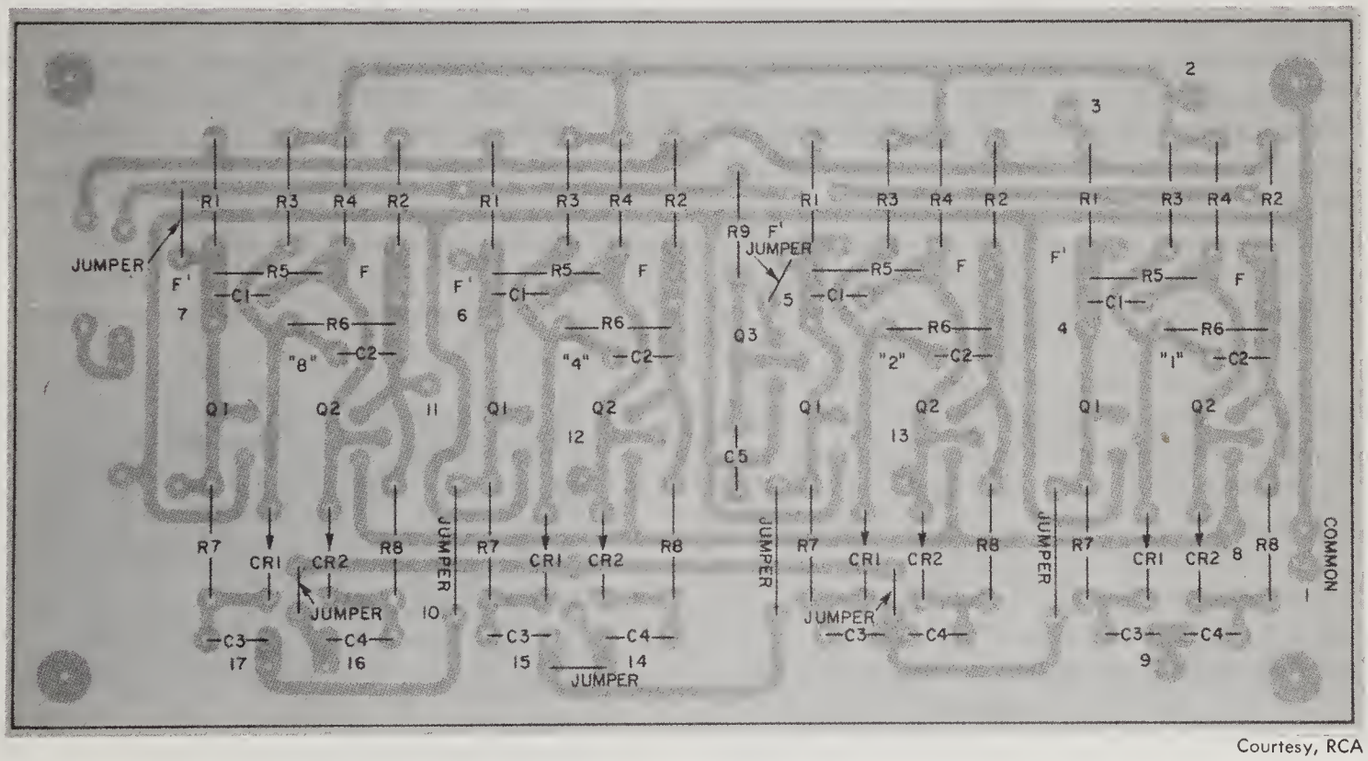
a. Short-circuited input to units counter.
b. Spurious reset pulse arriving simultaneously with the first input pulse (check with scope).
c. Short circuit on reset line.
d. Defect in units counter, such as a faulty transistor.

When all the Nixie tubes are dark continuously, they may not be receiving power. A voltmeter check should be made to determine if there is sufficent voltage at the Nixie tubes. The same possibility applies to incandescent-lamp display devices, Numitrons, and so on. If only one segment in a Numitron is dark continuously, the technician concludes that power is available but that a fault will be found in the circuitry for the affected segment. In other words, the filament segment might be burned out (open) or a short circuit might be found in the filament supply line. Or, the filament line might be normal, but a gating device might be defective. Integrated-circuit gates can be tested with a logic probe and logic pulser as illustrated in Fig. 5-20. In case the gate action tests normal, the trouble is most likely to be caused by subnormal pulse amplitude, absent pulses, or nonsimultaneity of pulses (mistimed pulses). These possibilities should be checked with a triggered-sweep oscilloscope. Note that adapter clip leads can be used with a logic pulser for applying a logic-high pulse simultaneously to the various inputs of an AND gate or for other tests requiring multiple logic-high inputs.



Courtesy, Hewlett-Packard

Fig. 5-20. Checking gate action with logic probe and logic pulser.



Courtesy, RCA

Fig. 5-19. Circuit-board layout for a decade counter.

2. Incorrect Readout Displayed

Common causes of incorrect readout are:

a. Open segment in a seven-segment display device, such as a Numitron tube (Fig. 5-3).
b. Defective gate in a bcd decoder, as in Fig. 5-13.
c. Open capacitor, such as C5 in Fig. 5-16.
d. Poor front-to-back ratio in a steering diode, such as CR1 in Fig. 5-17.
e. Leakage or a short circuit between circuit-board conductors (see Fig. 5-19).

3. Failure To Start Counting From Zero

Common causes of failure to start counting from zero are:

a. Defect in reset circuitry, such as a faulty inverter in Fig. 5-10.
b. Replacement diode connected in reversed polarity.
c. Malfunctioning AND gate in bcd decoder, as in Fig. 5-13B.
d. Distorted reset pulse; check with oscilloscope.
e. Open circuit-board conductor; trace pulses from point to point with scope.

4. Intermittent Operation

There are many possible causes of intermittent operation in display systems. Sometimes the trouble area can be narrowed down considerably by evaluation of the particular symptoms with respect to the block diagram and the schematic diagram for the digital equipment. In any case, it is usually helpful to monitor the system operation at various points with oscilloscopes and voltmeters. In turn, when the intermittent condition appears, the technician can check the monitoring instruments for missing pulses, bad-level pulses, spurious pulses, seriously distorted pulses, and incorrect voltage levels. Brief intermittents are the most difficult to track down because there may be insufficient time to observe the instrument readings and displays before normal operation is resumed. In such situations, it may be necessary to have several technicians observe the instruments so that brief operating irregularities can be located promptly.

Common causes of intermittent operation in display systems are:

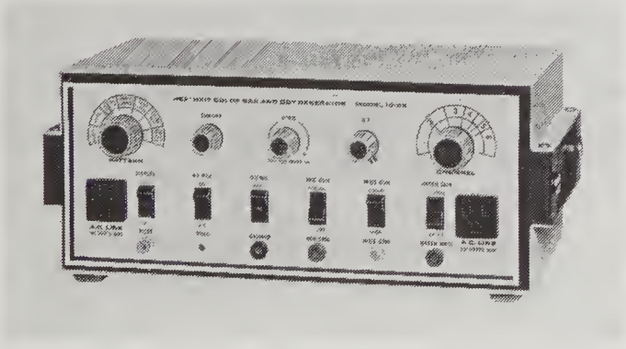
a. Cold-soldered joints and defective contacts; these cause the majority of intermittents. Check socket contacts of display devices.
b. An intermittent display device. For example, occasionally a burned-out filament segment in a display tube may make intermittent contact to its support.
c. An intermittent capacitor, such as C5 in Fig. 5-16.
d. A microscopic break in a circuit-board conductor; this is very likely to cause intermittent operation.
e. An intermittent IC; either mechanical or thermal intermittents may occasionally develop.

CHAPTER 6

Digital Logic in Electronic Instruments

Digital logic is utilized in various types of electronic instruments. As an example, the color-bar and dot generator shown in Fig. 6-1 employs logic circuitry to produce the patterns depicted in Fig. 6-2 on the screen of a television receiver. The generator contains a master-clock oscillator and various combinations of gates and flip-flops to develop the waveforms corresponding to the 12 screen patterns. Typical trouble symptoms that may be encountered in this type of generator are:

1. Video, but no sync-waveform output.
2. Bars missing from color pattern.
3. No vertical bars, dots, or crosshatch output.
4. No horizontal line, dots, or crosshatch output.
5. Erratic or intermittent operation.



Courtesy, Heath Co.

Fig. 6-1. A color-bar and dot generator that utilizes logic circuitry.

GENERAL DISCUSSION

An overview of the color-bar and dot generator function is shown in the block diagram of Fig. 6-3. A crystal-controlled master-clock oscillator generates a stable sine wave. In turn, this sine wave is shaped by succeeding stages and is then applied to a divider chain consisting of a series of flip-flops and multivibrators. The flip-flops divide the frequency of the clock signal into submultiples of the clock frequency. At various points along the divider chain, pulses with required repetition rates are picked off and applied to different AND, NOR, and OR gates. These gates combine the necessary pulses to form the required output waveforms. The clock frequency is 190.08 kHz, which is progressively divided down to 60 Hz.

It is helpful at this point to note the chief features of the generator operation. A divider-chain driver circuit clips the 190.08-kHz sine wave into a square wave. In turn, the repetition rate of this square wave is divided down for driving the various gate circuits and output switching circuitry. Outputs from the gates, the driver, and the clock oscillator are coupled to the pattern-selector switch. The various positions of this switch select the proper waveforms for display of particular patterns. To obtain a vertical-line display, the output from the clock and divider-chain driver is

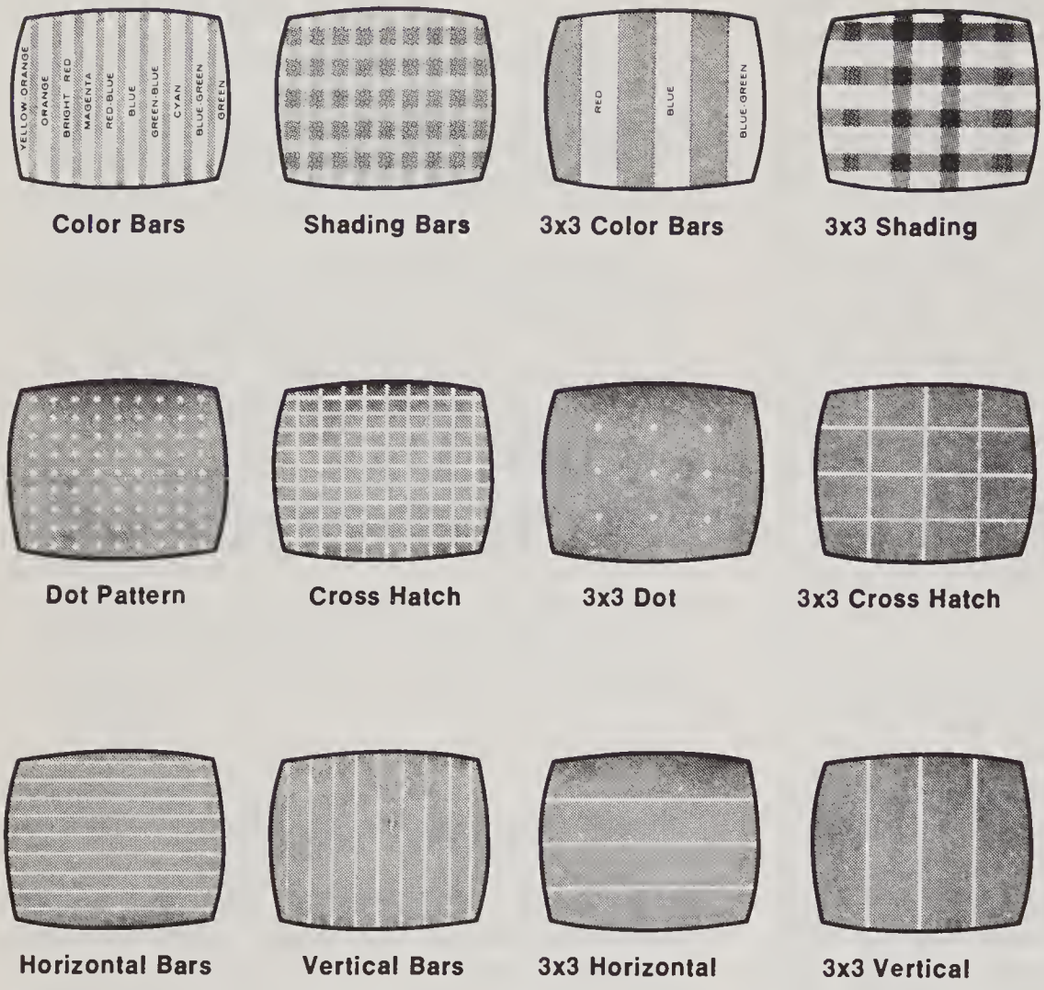


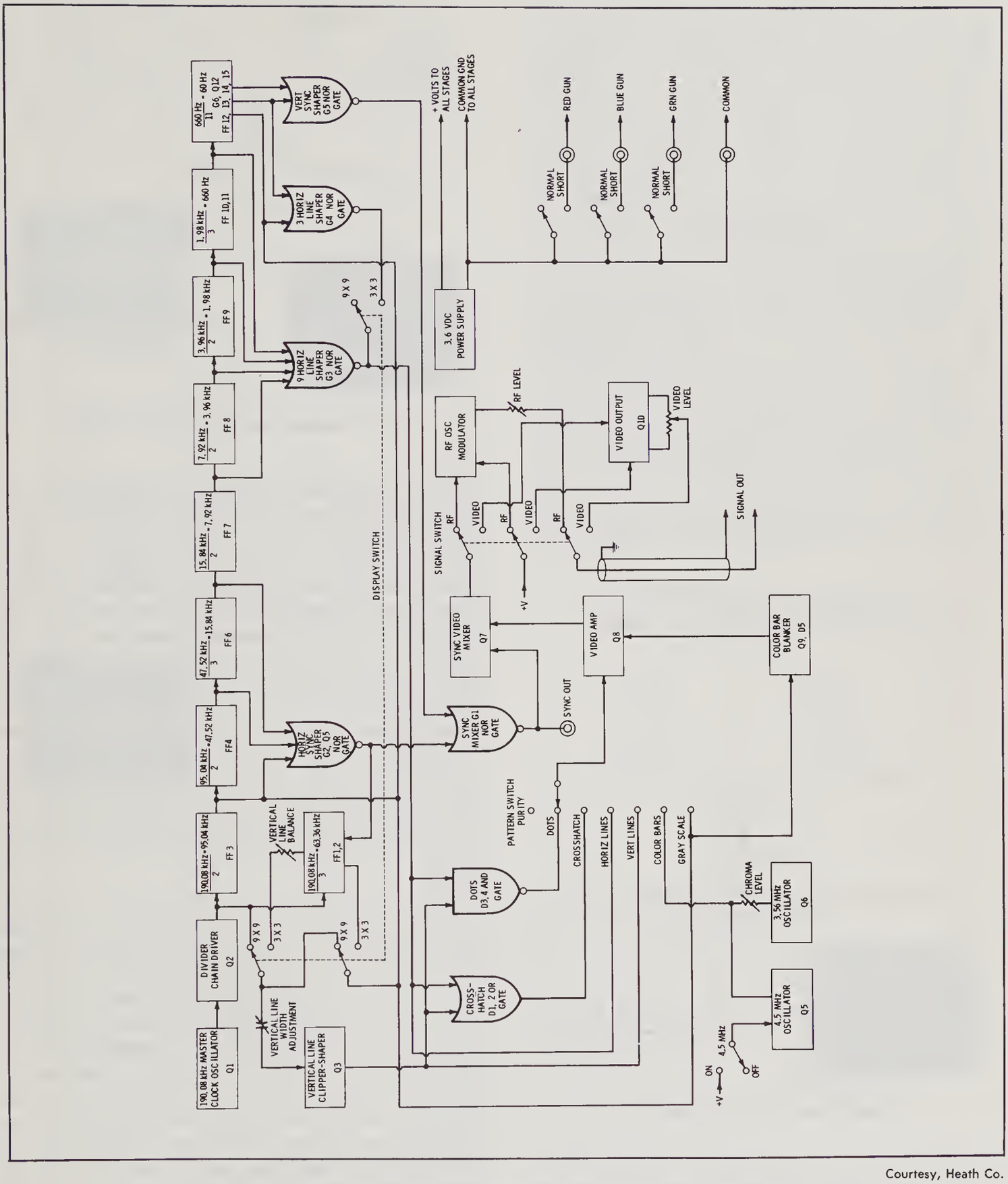
Fig. 6-2. Patterns produced by the generator in Fig. 6-1.

processed through the clipper-shaper stage, which differentiates the pulses. In this manner, a spike waveform is produced which will display a narrow vertical line on the picture-tube screen. This video pulse is combined with the sync waveform in the sync/video mixer circuit, as detailed subsequently. In turn, the required number of pulses per horizontal sweep period are combined with the sync waveform to display the chosen number of vertical lines.

Next, horizontal lines are obtained by feeding outputs from the divider chain to a NOR gate. In turn, a pulse output is obtained that displays a narrow horizontal line on the picture-tube screen. This pulse is combined with the sync waveform in the sync/video mixer circuit. Thus, the required number of pulses per vertical sweep period are combined with the sync waveform to display the chosen number of horizontal lines. Next, in order to display a crosshatch pattern, the horizontal and vertical line pulses are combined in an OR gate. Accordingly, the output from the OR gate comprises both the vertical and the horizontal line pulses. This waveform displays a crosshatch pattern on the screen of the television receiver. To display a dot pattern, an AND gate is utilized to combine the vertical and horizontal pulse signals. Since both vertical and horizontal pulses must be present at the input of the AND gate to produce an output, the gate develops an output pulse only at the times that the vertical and horizontal lines cross. In turn, a dot pattern is displayed on the television-receiver screen. To display a gray-scale pattern, pulses are combined to form a wide-bar crosshatch pattern. In turn, the bars are superimposed at their intersections so that a change in gray shade is displayed.

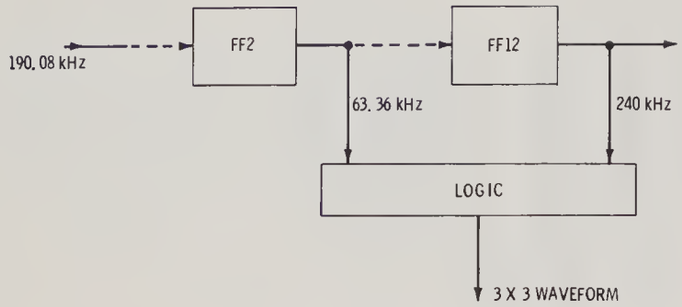
FUNCTIONAL DESCRIPTION OF COLOR-BAR AND DOT GENERATOR

With reference to Fig. 6-4, the 63.36-kHz pulse output from FF2 and the 240-Hz pulse output from FF12 are combined to provide a waveform

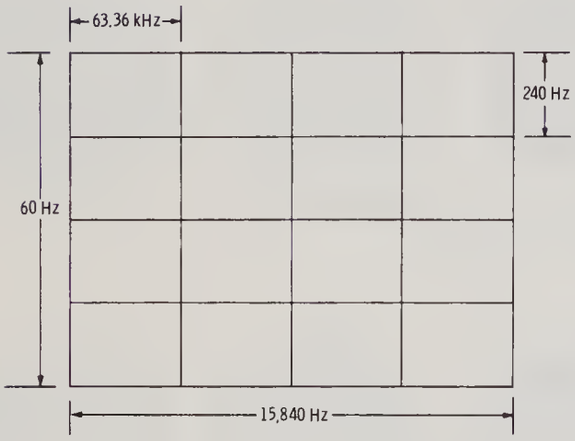


Courtesy, Heath Co.

Fig. 6-3. Block diagram showing color-bar and dot generator functions.

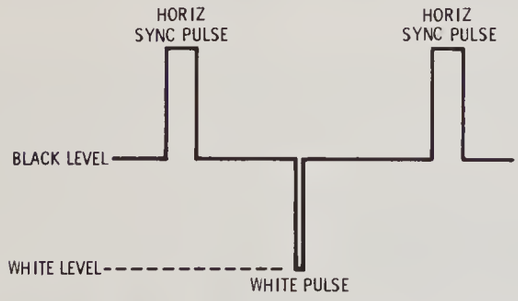


(A) Block diagram.



(B) Frequency and display relationship.

Fig. 6-4. Formation of the basic 3 × 3 display.

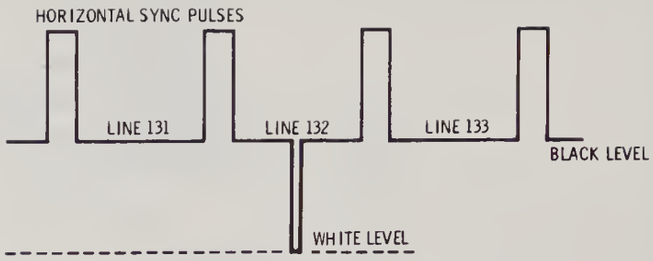


(A) A single pulse placed half-way between horizontal sync pulses.

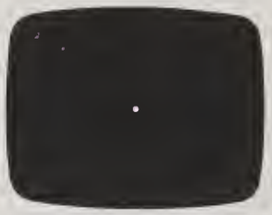
(B) Successive pulses provide a vertical-line display.

Fig. 6-5. Display of a vertical white line.

that produces a type of display called a 3 × 3 pattern on the picture-tube screen. Observe that the actual horizontal-scanning frequency employed is 15,840 Hz, and 63.36 kHz is four times this



(A) Narrow pulse is inserted in line 132.

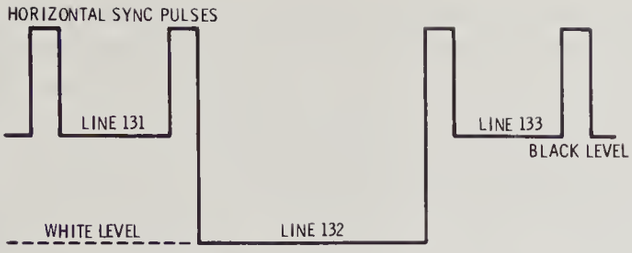


(B) Waveform provides a single-dot display.

Fig. 6-6. Display of a single dot at center screen.

horizontal-scanning frequency. Similarly, the vertical-scanning frequency is 60 Hz, and 240 Hz is four times the vertical-scanning frequency. Line and dot patterns are displayed by means of pulse waveforms. As an illustration, consider a waveform that will provide a vertical, white line down the center of the picture-tube screen, as depicted in Fig. 6-5. On each successive scan, a negative pulse is inserted halfway between horizontal sync pulses. Fig. 6-5A shows that this pulse extends from the black level to the white level on the video waveform. It produces a white dot on each horizontal scan by turning on the scanning beam as it reaches the halfway point on the screen. Since a white dot is displayed on each horizontal scan, a vertical white line is displayed on the entire screen.

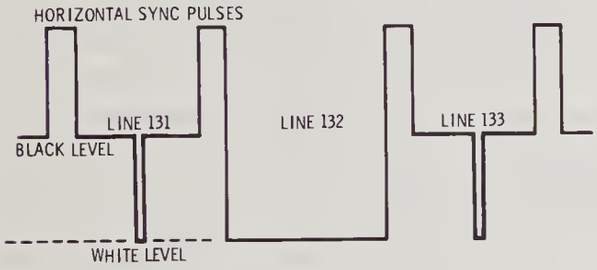
Next, consider the waveform that is required to display a single white dot in the center of the picture-tube screen. Referring to Fig. 6-6, a pulse is inserted in only one horizontal-scanning line—the line that scans through the center of the screen. Thus, on the 132nd horizontal scan, a 0.25-μs pulse is inserted which extends from the black level to the white level in the video waveform. In turn, a white dot is displayed in the center of the screen. Not shown in Fig. 6-6 are vertical sync pulses which are necessarily included to lock the white dot in position on the screen. Recall that a vertical sync pulse occurs every 1/60 second. Dividing 15,840 by 60, it is apparent that 264 horizontal lines occur for each



(A) Wide pulse is inserted in line 132.

(B) Waveform provides a single-line display.

Fig. 6-7. Displaying a single horizontal white line.



(A) Vertical and horizontal single-line waveforms are combined.

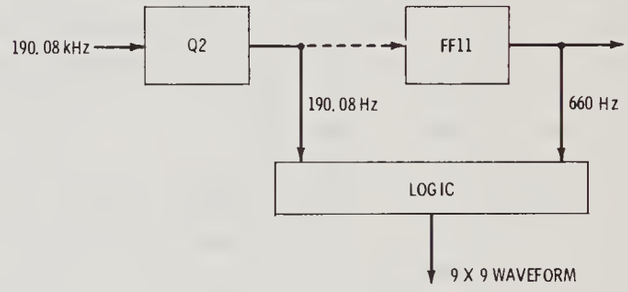
(B) A basic "crosshair" pattern.

Fig. 6-8. Displaying a "crosshair" pattern.

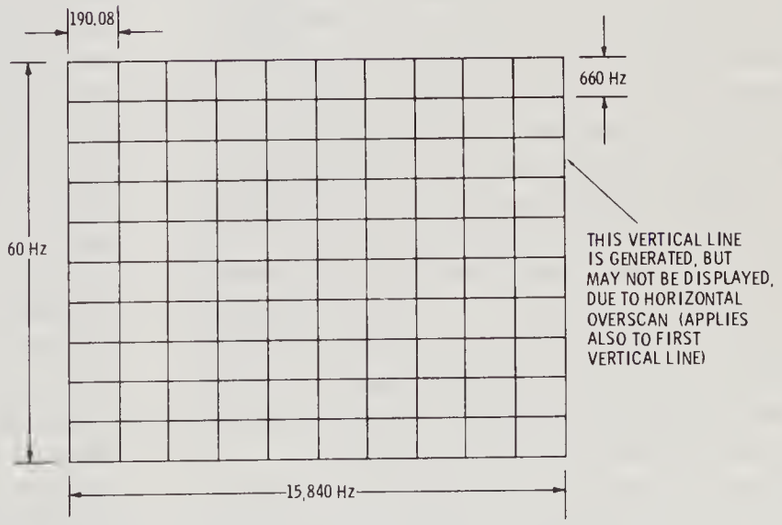
vertical scan. Sync pulse generation and routing are discussed subsequently.

To display a single horizontal line on the picture-tube screen, the same general type of waveform is employed, except that a 60-μs pulse is inserted as shown in Fig. 6-7. Note that although a horizontal line occupies a total period of 63.5 μs, the horizontal sync pulse reduces the effective forward-scan time. A period of 5.1 μs is lost on each horizontal-retrace interval, during the occurrence of the horizontal-sync pulse. Observe next that in order to display a "crosshair" pattern through the center of the picture-tube screen, as depicted in Fig. 6-8, a combination of single vertical-line and single horizontal-line waveforms is utilized.

Consider next how the basic 9×9 display is produced. Referring to Fig. 6-9, the 190.08-kHz signal from Q2 and the 660-Hz signal from FF11 are combined to display a basic pattern of nine horizontal elements and nine vertical elements. With reference to Fig. 6-3, note that the combined vertical and horizontal sync pulses and the pattern



(A) Block diagram.



(B)Display frequency relationships.

Fig. 6-9. Formation of the basic 9×9 display.

waveform from the video amplifier are combined in the sync/video mixer stages to provide the composite video signal. This composite video signal is then coupled to the video-output stage or to the rf modulator, depending on the setting of the signal switch. Note that the video-output stage supplies a composite video signal for injection directly into the video circuits of a television receiver. The rf oscillator provides a vhf carrier that is modulated by the video signal and that can be tuned through television channels 2 to 6.

At this point, it is helpful to briefly consider the characteristics of the flip-flops that are employed in Fig. 6-3. These are JK flip-flops, as mentioned in the preceding chapter. Each JK flip-flop has two outputs, which are denoted Q and $\overline{Q}$ (Q and NOT Q) Each flip-flop also has three input terminals, called S (set), C (clear), and T (trigger). These inputs can be utilized in an arrangement such that a pulse applied to the trigger input will or will not change the state of the flip-flop, depending on the ON conditions at the set and clear terminals. In addition, a P (preset) terminal provides a means for returning the flip-flop to a specified state, independently of the trigger input. If both the S and C terminals are grounded, the output will be ON after two pulses have been applied to the trigger input—this is called a divide-by-two action.

Fig. 6-10 depicts a JK flip-flop with a preset input terminal. It is often called a clocked JK flip-flop. The Q and $\overline{Q}$ outputs are called 1 and 0 outputs. Note also that the set input is called a J input, and the reset input is called a K input. The trigger input is called the clock (C_p) input. To repeat an important fact, when a clocked JK flip-flop is utilized, both the set and reset inputs can be made logic-low or logic-high in any combination, and the output will not change until a clock (trigger) pulse is applied to the flip-flop. Observe that the preset input permits placing the JK flip-flop in a known state whenever a positive-going pulse is applied to the preset input. The flip-flop responds to a preset pulse by forcing the paralleled transistors into conduction so that the Q output is forced to be logic-low. Preset action is sometimes called a priority response because it overrides the set, reset, and trigger inputs. A preset input is alternatively called a clear input.

Flip-flops FF1 and FF2 in the block diagram of Fig. 6-3 are connected to divide by three as shown in Fig. 6-11. To start, let us assume that the Q output of FF1 is at a 1 level and that the Q output of FF2 is at the 0 level. When a trigger pulse is applied, both flip-flops change state. This places the S and C inputs of FF1 at a 1 level. The next trigger pulse causes FF2 to change state. FF1 was prevented from changing state by the 1 level at its S and C inputs. These responses are summarized in the counting-sequence table. Observe that the first trigger pulse causes both flip-flops to reverse their states and that the second trigger pulse causes only FF2 to change state. Again, the third trigger pulse causes only FF1 to change state, and the flip-flops are then back in their starting condition.

Observe that the trigger pulse is applied simultaneously at the T inputs of FF1 and FF2 in Fig. 6-11. By the time that FF2 changes state, the trigger pulse no longer affects that state of FF1. Note that the third trigger pulse causes FF1 to change state but that FF2 is unaffected because of the 1 level at the C input. Proceeding to Fig. 6-12, consider how FF12, FF13, FF14, and FF15 are arranged to divide by eleven. Repeating a basic point, to set a flip-flop means to place the flip-flop in its $Q = 1$ state; to reset a flip-flop means to place the flip-flop in its $Q = 0$ state; to preset a flip-flop means to place the flip-flop in a specified condition prior to going into operation. When a flip-flop has been preset, its circuit action will then start from the preset condition.

Referring to Fig. 6-12, when a 1-level pulse is applied to the preset inputs, the Q outputs of all four flip-flops are placed at the 0 level. Correspondingly, the $\overline{Q}$ outputs of all four flip-flops are placed at the 1 level. Note that NOR gate G6 will produce a positive output pulse only when all four of its inputs are at the 0 level, which occurs only on the 11th pulse (or the 10th state). In other words, in this 10th state, G6 receives a $Q = 0$ output pulse from FF12, a $\overline{Q} = 0$ output pulse from FF13, a $Q = 0$ output pulse from FF14, and a $\overline{Q} = 0$ output pulse from FF15. Next, the square-wave output from G6 is differentiated by the 470-pF capacitor and the 4700-ohm resistor, thereby producing a positive pulse on the leading edge and a negative pulse on the trailing edge of the square wave. This negative pulse cuts off Q12 and causes a rise in collector voltage. This voltage rise is applied to the preset inputs of all four flip-flops and returns them to 0-0-0-0. Thus, the configuration divides by eleven.

Sync pulses are generated in associated sec-

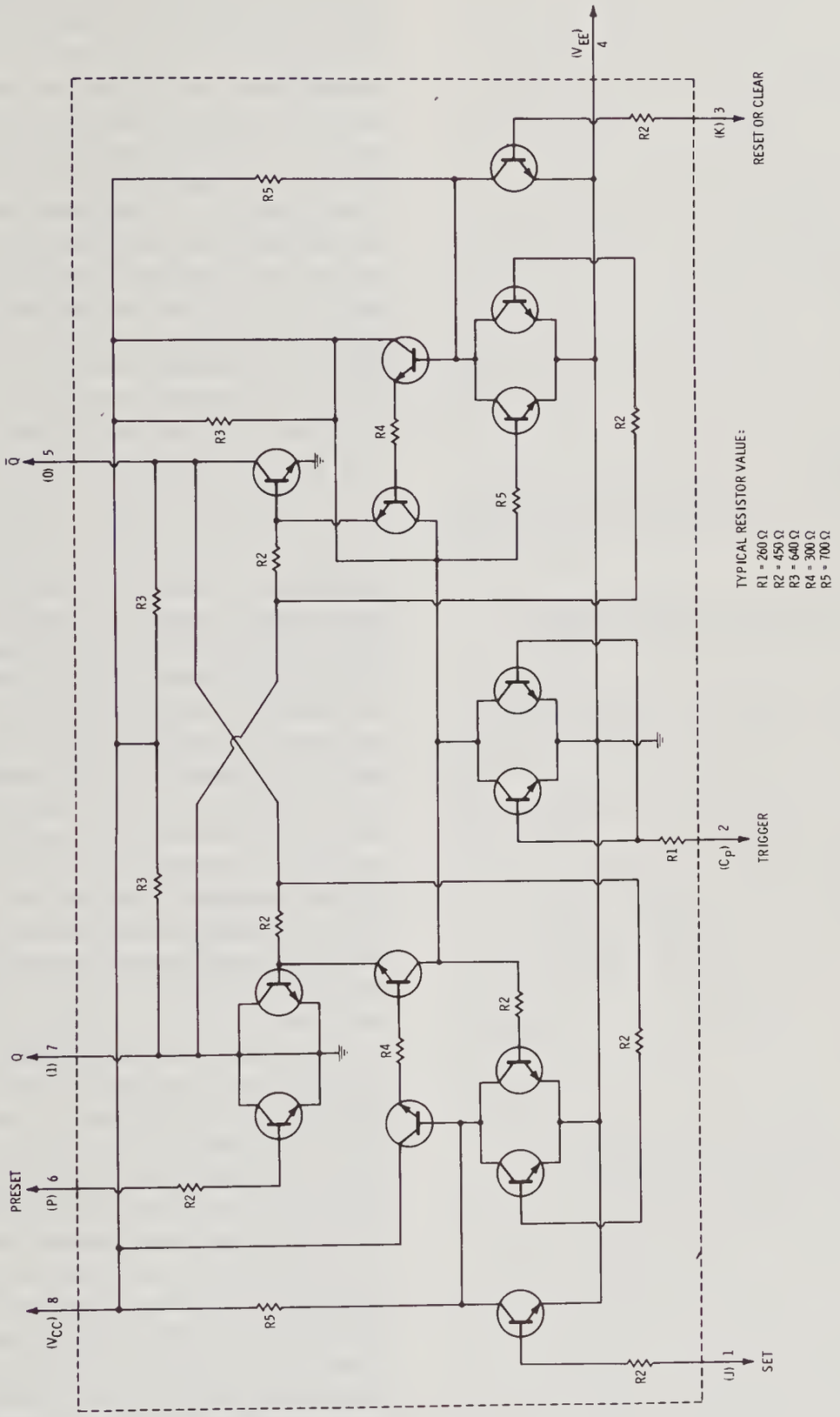
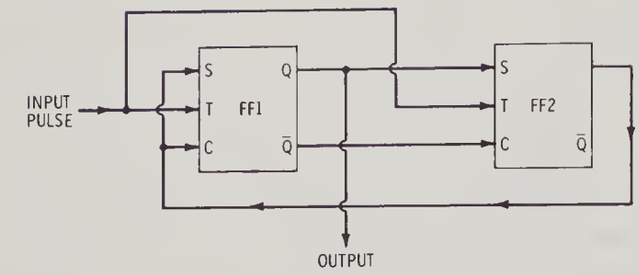
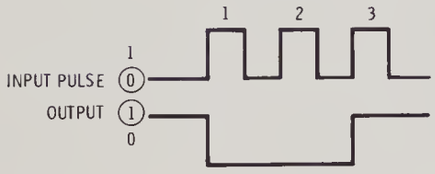


Fig. 6-10. A JK flip-flop with a preset input terminal.



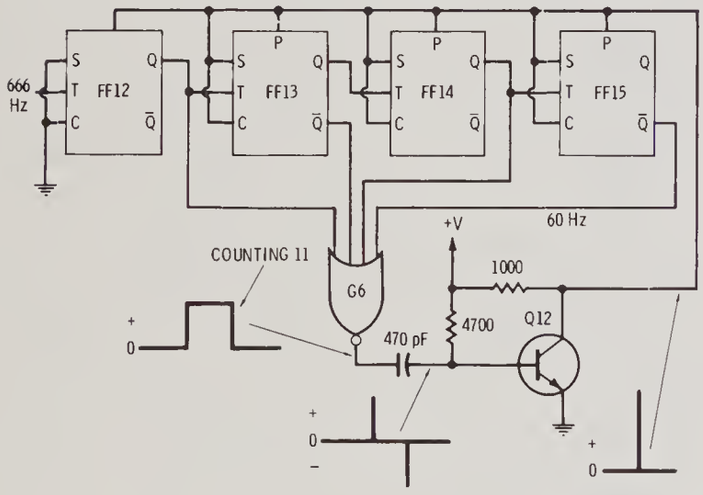
(A) Block diagram.



COUNTING SEQUENCE		
PULSE	FF1	FF2
	1	0
1	0	1
2	0	0
3	1	0

(C) Counting-sequence table.

Fig. 6-11. Plan of the divide-by-three logic configuration.



(A) Block diagram.

PULSE	FF12	FF13	FF14	FF15
0	0	0	0	0
1	1	0	0	0
2	0	1	0	0
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1

(B) Counting-sequence table.

Fig. 6-12. Plan of the divide-by-eleven logic configuration.

tions of the generator and are combined with the 3×3 or 9×9 patterns. With reference to the expanded block diagram for the generator shown in Fig. 6-13, the outputs from FF3, FF4, and FF5-FF6 are fed into the horizontal-sync-shaper arrangement comprising NOR gate G2 and transistor Q5. A simplified block diagram for the horizontal-sync shaper section is depicted in Fig. 6-14. Observe that Q5 may be considered as an added input to G2, inasmuch as their outputs are paralleled. When all inputs to G2 and Q5 are 0, a 1 output is produced by their paralleled output lead. This 1 output is a horizontal-sync pulse, and it remains on the output lead for the same period that all the inputs are zero. This is a period of 5.25 μs. Waveform relationships at the inputs and outputs of the horizontal-sync section are shown in Fig. 6-15. Troubleshooting procedures for loss of horizontal sync generally include observing these waveforms with a triggered-sweep oscilloscope.

Again with reference to Fig. 6-13, the vertical-sync pulse is formed by feeding the outputs from FF13 and FF15 into the vertical-sync shaper, NOR gate G5. The resulting 60-Hz vertical-sync is 252 μs wide. The vertical- and horizontal-sync pulses are mixed in NOR gate G1 to form the composite sync waveform. Note that because the horizontal-scanning frequency of 15,840 Hz is evenly divisible by the vertical-scanning frequency of 60 Hz, interlaced scanning is not provided. Also, since the vertical-sync pulse has no serrations, the sync signal is nonstandard in this respect. Nevertheless, the simplified sync waveform serves its purpose adequately for display of line, dot, and bar patterns.

It is helpful at this point to consider the expanded block diagram of Fig. 6-13 in somewhat greater detail. Transistor Q1 operates as a crystal-controlled 190.08-kHz sine-wave oscillator. This sine-wave voltage is coupled by capacitor C4 to the base of transistor Q2. Note that Q2 operates as a buffer stage to prevent excessive loading of the clock oscillator; it also operates as a clipper to square off the sine-wave signal. Next, the square-wave output from Q2 follows three paths. The first path couples the signal through variable capacitor C5 to the base of transistor Q3. In turn, the square wave becomes differentiated into positive and negative pulses. The positive pulses are amplified by Q3 and are processed into vertical-line, crosshatch, and dot waveforms.

Observe next in Fig. 6-13 that the master-clock signal proceeds through R8 and C6 to the trigger input of FF1 and FF2. This section forms the pulse output for the basic 3 × 3 display. The third path is through R7, which couples the 190.08-kHz signal to the first flip-flop in the main divider chain. Thus, the signal passes through the divider chain consisting of FF3 through FF15. The divider chain then divides the signal by 2, 3, or 11, to provide all the other signals for development of the various generator outputs. As noted above, outputs from FF3, FF4, and FF5-FF6 are coupled to the horizontal-sync-shaper NOR gate consisting of G2 and Q5. When all of the input signals to this NOR gate are at 0, a narrow horizontal-sync pulse is produced by the gate. Similarly, outputs of FF13 and FF15 are fed to the vertical-sync-shaper NOR gate G5 in order to form the vertical sync pulse.

From their respective sync shapers, the vertical- and horizontal-sync pulses are fed to NOR gate G1. This gate combines the input pulses to form the composite sync signal. This sync signal is also coupled to the sync/video mixer circuit. Basically, a sync shaper operates like a clipper. It clips the applied pulses to a predetermined amplitude and, in so doing, improves the rise time of the pulse. Clipping also ensures that the output pulses have flat tops, whereas the input pulses may tend to have pointed or rounded tops.

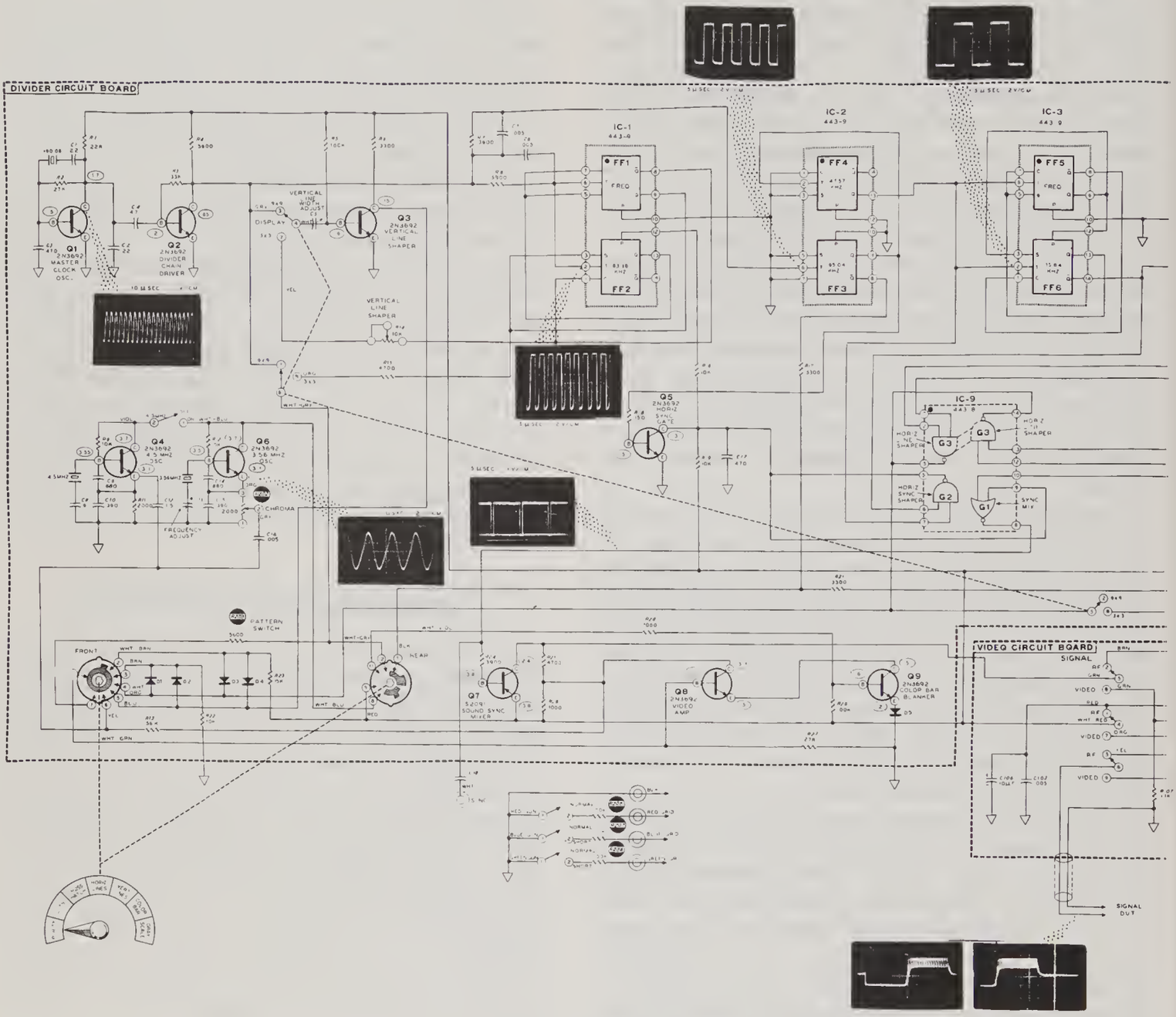
To provide a separate, variable video signal output, the output of transistor Q7 is applied through the signal switch and through capacitor C105 to the base of video-output transistor Q10, which operates as a phase splitter. Equal-value resistors R102 and R103 in the emitter and collector circuits of Q10 provide identical video signals of opposite polarity. These signals are then applied to opposite ends of the video-level control, R204. When the wiper of R204 is at the center of its range, the signal output is at a minimum. In turn, moving the wiper toward either end of its range will provide a variable-amplitude video signal with either positive or negative polarity. The sync and video signals are combined by Q7, Q8, and Q9. Note that Q9 is cut off only on color blanking. The video signal from lug 10 of the pattern switch is applied to the base of Q8. In turn, the output from video-amplifier transistor Q8 is developed across resistor R26. This resistor is also part of the load resistance for video-sync mixer transistor Q7.

When the negative-going sync pulse is applied to the base of Q7, the pnp transistor is driven into saturation. Thus, the collector is clamped to the power-supply voltage. This voltage completely overrides the video signal applied at the junction of R25 and R26 from video amplifier Q8. The resulting signal at the collector of Q7 is a combination of the sync and video signals. A Hartley oscillator circuit, consisting of Q11, C107-C108, and the printed-circuit coil L2, generates a signal in the range from 50 to 100 MHz to cover channels 2 through 6. To provide a combined rf and video signal, the sync/video output of Q7 is mixed with the output of Q11 at the anode of modulation diode D101. As the forward bias on the diode is increased by the video/sync signal, the effective resistance of the diode decreases. This results in a greater percentage of rf appearing across the rf level control R205. In turn, the wiper of rf-level control R205 picks off a portion of this modulated signal.

TROUBLESHOOTING TECHNIQUES

Digital-equipment servicing data may provide charts of specified test points and voltage values, as exemplified in Fig. 6-16. Key waveforms may also be specified, as seen in Fig. 6-13. Note that the operation of the complete divider chain can be checked by connecting a scope to the generator sync-output jack. There is normally a 15,840-kHz pulse-train voltage and a 60-Hz pulse-train voltage at this point. If the 15,840-kHz waveform is missing, it would be logical to conclude that there is a defect in flip-flops FF3 through FF6, or in, G2, Q5, or G1. On the other hand, if the 60-Hz waveform is missing, this indicates that there is a defect in flip-flops FF7 through FF15, or in, G6, Q12, G5, or G1.

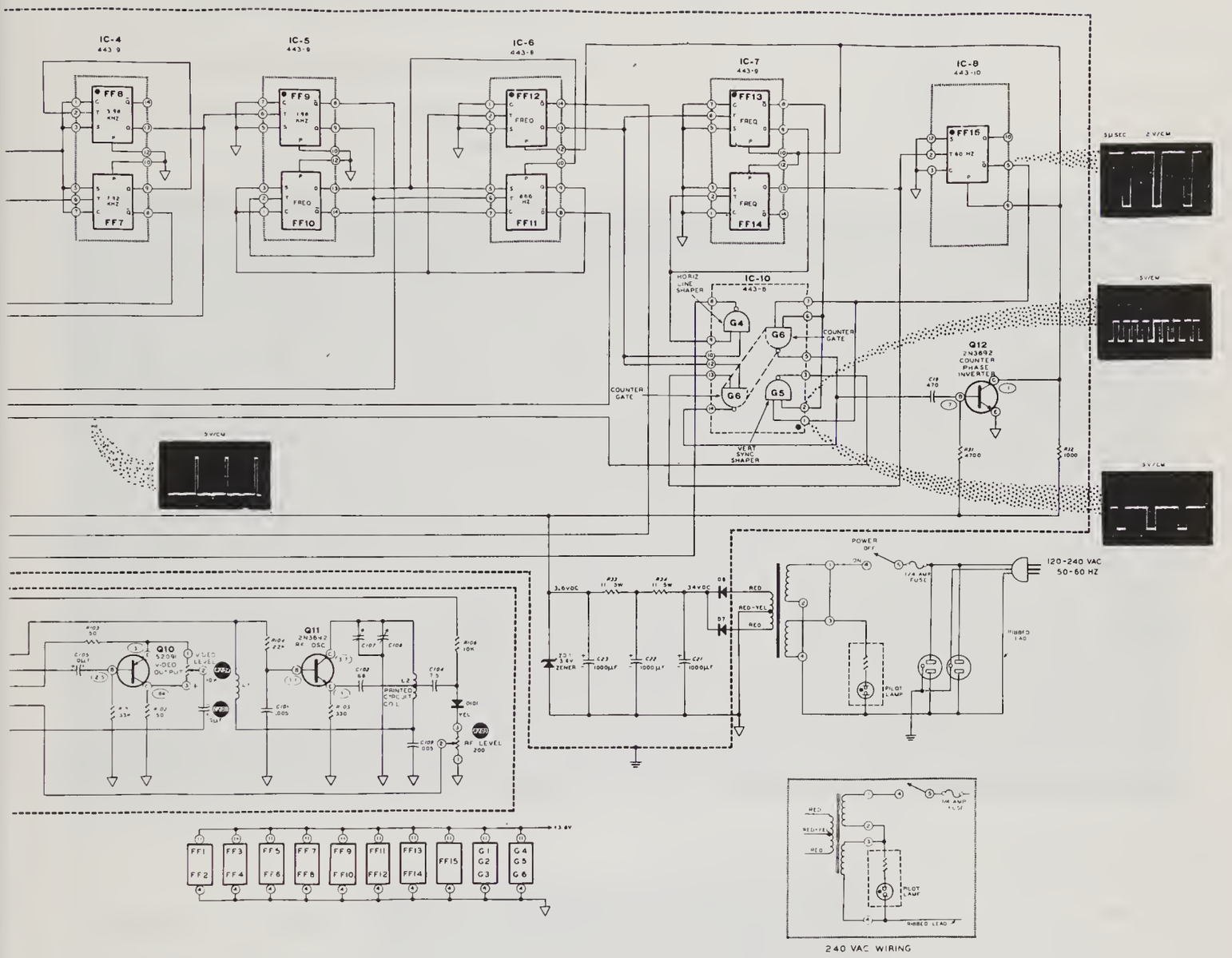
To check an IC in the divider chain, connect a scope to the trigger input (T) of the IC and test for the presence of a pulse waveform. If no pulse is present, check the Q and $\overline{Q}$ outputs of the preceding IC. If an IC has a normal input waveform but no output, there is either a poor connection, no supply voltage, or an internal defect in the IC. Note that when identical ICs are utilized in a chain, they can be interchanged for a crosscheck (see Fig. 6-17). As explained previously, tests can also be made with a logic probe and pulser to identify a faulty IC. A logic clip may also be utilized to test ICs.



NOTES:

1. RESISTOR AND CAPACITOR NUMBERS ARE IN THE FOLLOWING GROUPS:
   - 1-99 PARTS ON THE DIVIDER CIRCUIT BOARD.
   - 100-199 PARTS ON THE VIDEO-RF CIRCUIT BOARD.
   - 200-299 PARTS ON THE CHASSIS.
2. ALL RESISTORS ARE 1/2 WATT UNLESS MARKED OTHERWISE. RESISTOR VALUES ARE IN OHMS (K=1000, MEG=1,000,000).
3. ALL CAPACITOR VALUES LESS THAN 1 ARE IN µF. VALUES OF 1 AND ABOVE ARE IN pF UNLESS MARKED OTHERWISE.

Fig. 6-13. Expanded block diagram of



4. ⬭ THIS SYMBOL INDICATES A POSITIVE DC VOLTAGE MEASUREMENT, TAKEN WITH AN 11 MEGOHM INPUT VOLTMETER, FROM THE POINT INDICATED TO CHASSIS GROUND. VOLTAGES MAY VARY ±20%.

5. SUPPLY VOLTAGES AND GROUND POINTS TO THE INTEGRATED CIRCUITS ARE SHOWN IN A SEPARATE DRAWING ON THE SCHEMATIC.

6. VOLTAGE READINGS WERE TAKEN WITH THE PATTERN SWITCH IN COLOR BAR POSITION AND ALL OTHER CONTROLS TURNED FULLY CLOCKWISE EXCEPT AS INDICATED.

Courtesy, Heath Co.

Heath color-bar and dot generator.

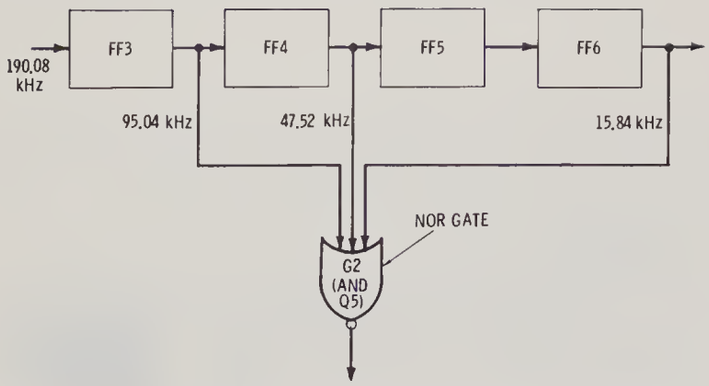


Fig. 6-14. Block diagram of horizontal sync-pulse section.

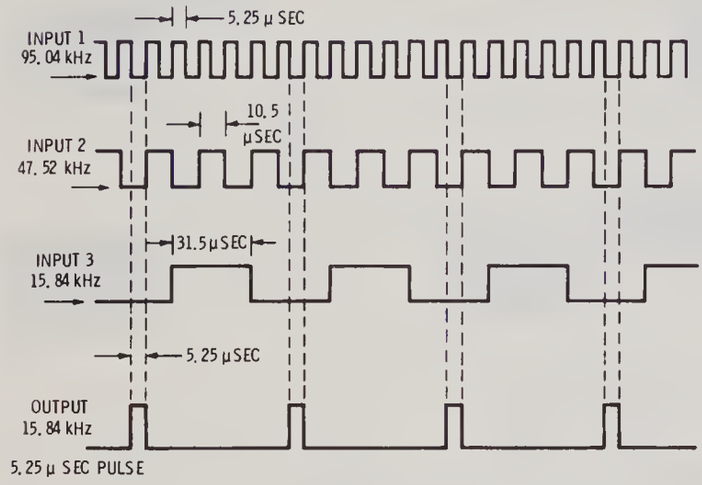


Fig. 6-15. Horizontal sync-pulse generation.

1. Video But No Sync Waveform Output

When there is video output but no sync, pulse tracing with the scope is the best preliminary approach. After the trouble area is localized, dc-voltage measurements can be used to narrow down the possibilities. Waveforms for this example are shown in Fig. 6-13, and voltages are specified in Fig. 6-16. In case that service data is not available for the particular digital equipment being serviced, it is sometimes possible to make comparison tests on similar equipment that is in normal operating condition. Common causes of video output with no sync are:

a. Defective sync-mixing gate, such as G1 in Fig. 6-13.
b. Faulty transistor in video-sync mixing section, such as Q7 in Fig. 6-13.
c. IC failure in sync channel.
d. Short circuit between circuit-board conductors.
e. Leaky or shorted capacitor, such as C17 in Fig. 6-13.
f. Resistor far off value, such as R18 in Fig. 6-13 (not likely, but possible).

2. Bars Missing From Color Pattern

Common causes of a rainbow color display with no dark bars are:

a. Open or shorted color-bar blanker diode, such as D5 in Fig. 6-13.
b. Defective color-bar blanker transistor, such as Q9 in Fig. 6-13.
c. Defective switch contacts in keying-pulse circuit.
d. Resistor far off value, such as R28 in Fig. 6-13 (not likely, but possible).

3. No Vertical Bars, Dots, or Crosshatch Output

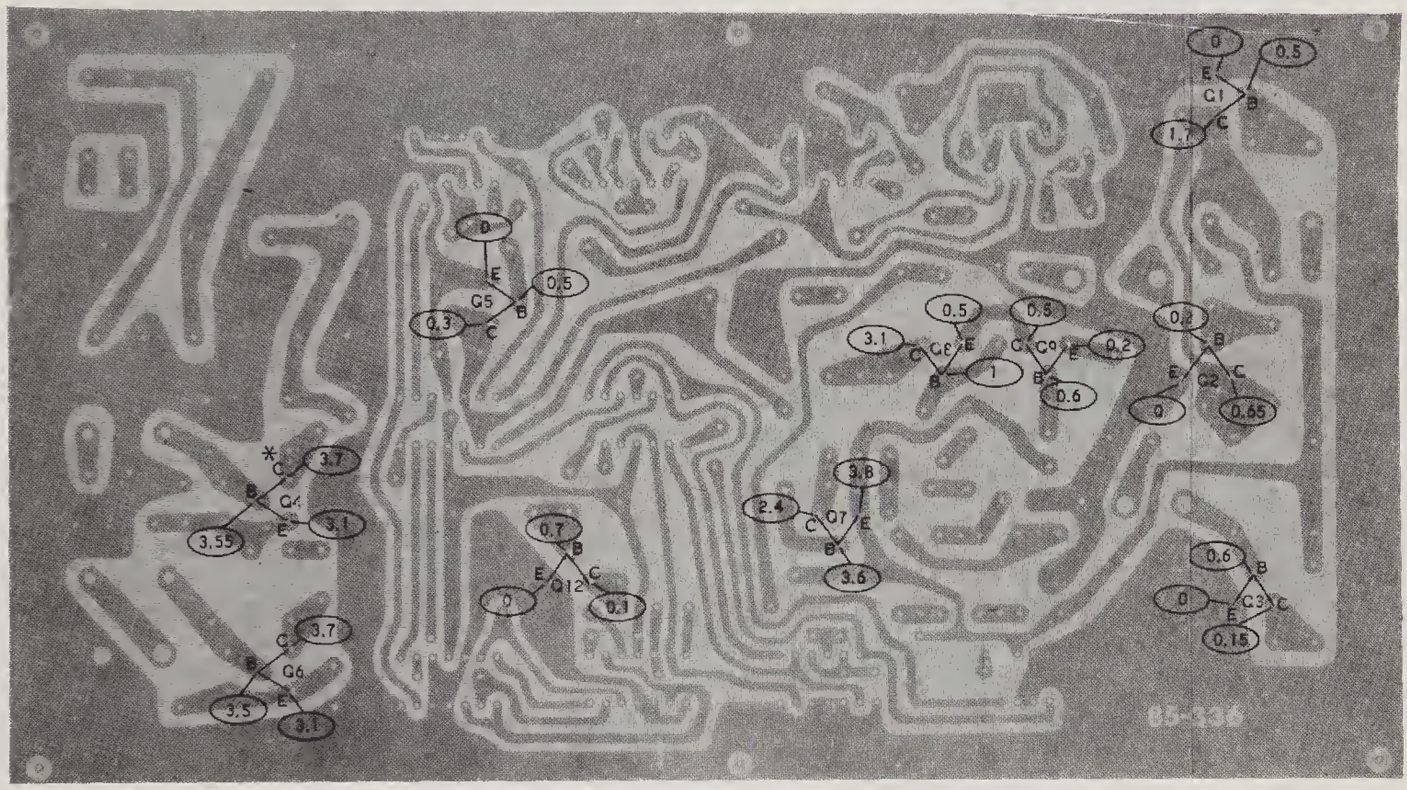
This trouble symptom indicates that the trouble originates in the vertical pulse channel. Possible causes are:

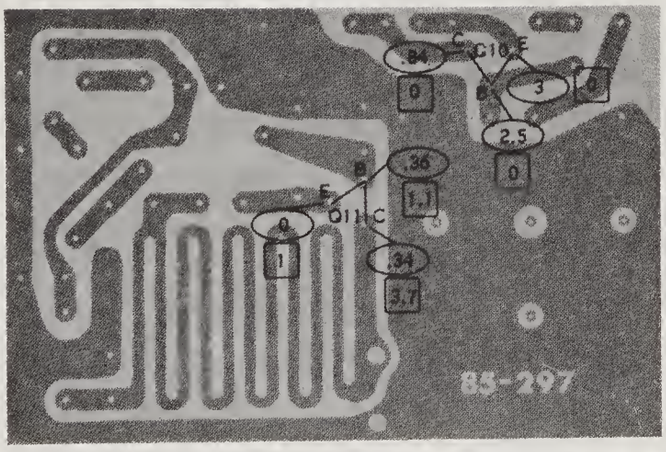
a. Defective vertical-line-shaper transistor, such as Q3 in Fig. 6-13.
b. Vertical-line-width capacitor misadjusted or defective (C5 in Fig. 6-13).
c. Poor contact in display switch.
d. Resistor far off value (R5 or R6 in Fig. 6-13).
e. Broken circuit-board conductor in vertical-pulse channel.

4. No Horizontal Lines, Dots, or Crosshatch

When there are no horizontal lines, dots, or crosshatch, and the vertical lines and sync are normal, the required source signals are present but are not being normally processed into patterns. Pulse tracing with the scope is the best preliminary approach. Possible causes of this trouble symptom are:

a. Horizontal-line-shaper NOR gate defective, such as G3 or G4 in Fig. 6-13.
b. Defective gate socket or cold-soldered terminal connection.
c. Poor switch contact(s).
d. Broken circuit-board conductor, or short circuit between conductors.





Courtesy, Heath Co.

Fig. 6-16. Example of specified test points and voltage values.

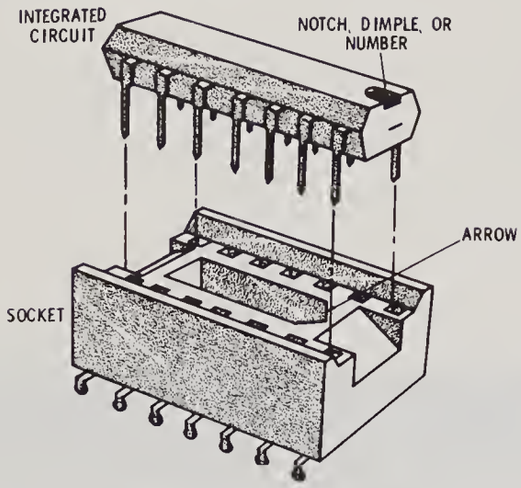


Fig. 6-17. IC must be correctly inserted and pressed fully down into socket.

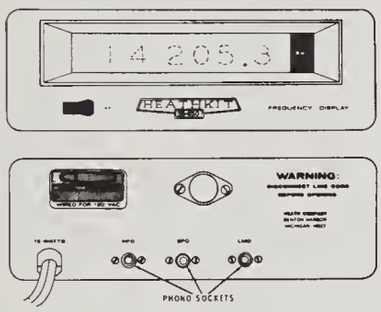
5. Erractic or Intermittent Operation

Erratic or intermittent operation is caused by the same basic faults as those explained above, except that the failure is marginal or the trouble condition is intermittent. Common causes are:

a. Power-supply voltage subnormal or fluctuating.
b. Defective output cable.
c. Transistor with collector leakage, such as Q2 in Fig. 6-13.
d. Marginal quartz crystal (not likely, but possible).
e. Abnormally high power-supply ripple.

CHAPTER 7

Digital Frequency Display Equipment



Courtesy, Heath Co.

Fig. 7-1. Front and rear views of digital frequency display unit.

Digital frequency display equipment represents a comparatively sophisticated form of instrumentation. Fig. 7-1 shows the front and rear views of a digital frequency display unit that operates in combination with amateur radio receivers and with five-band transceivers covering the 3- to 30-MHz range. It functions by determining the received frequency with an accuracy of ±0.1 kHz and displays the value of this frequency on six display tubes. As will be explained in greater detail subsequently, a digital up/down counter is

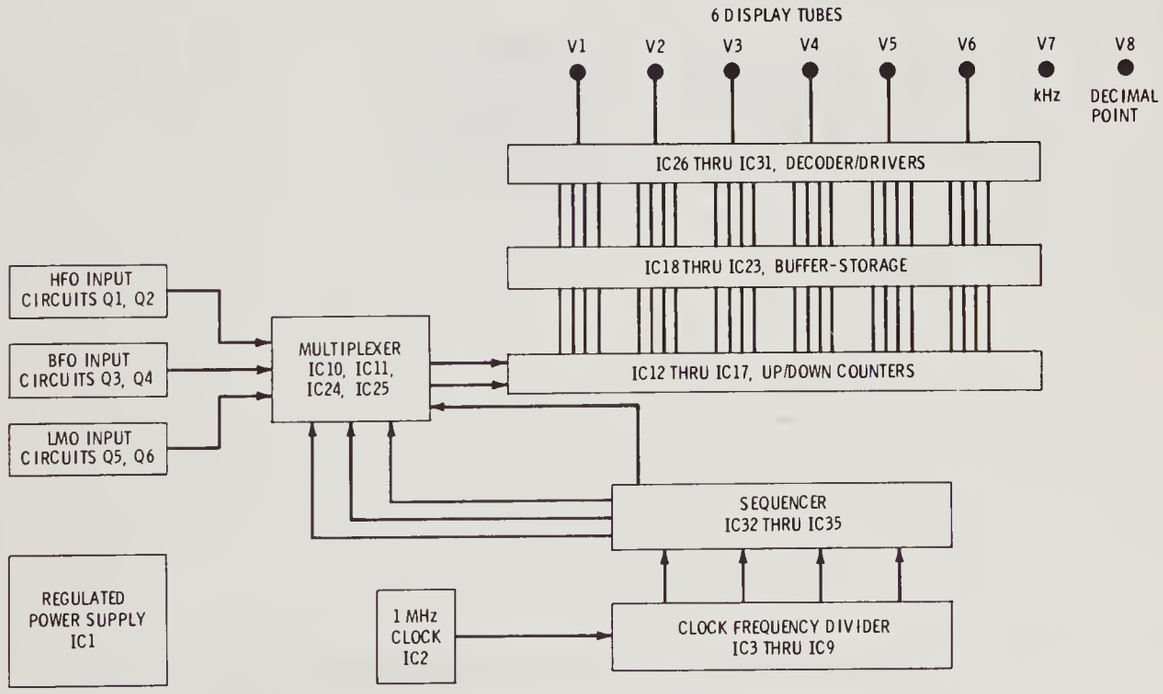


Fig. 7-2. Block diagram of the digital frequency display unit.

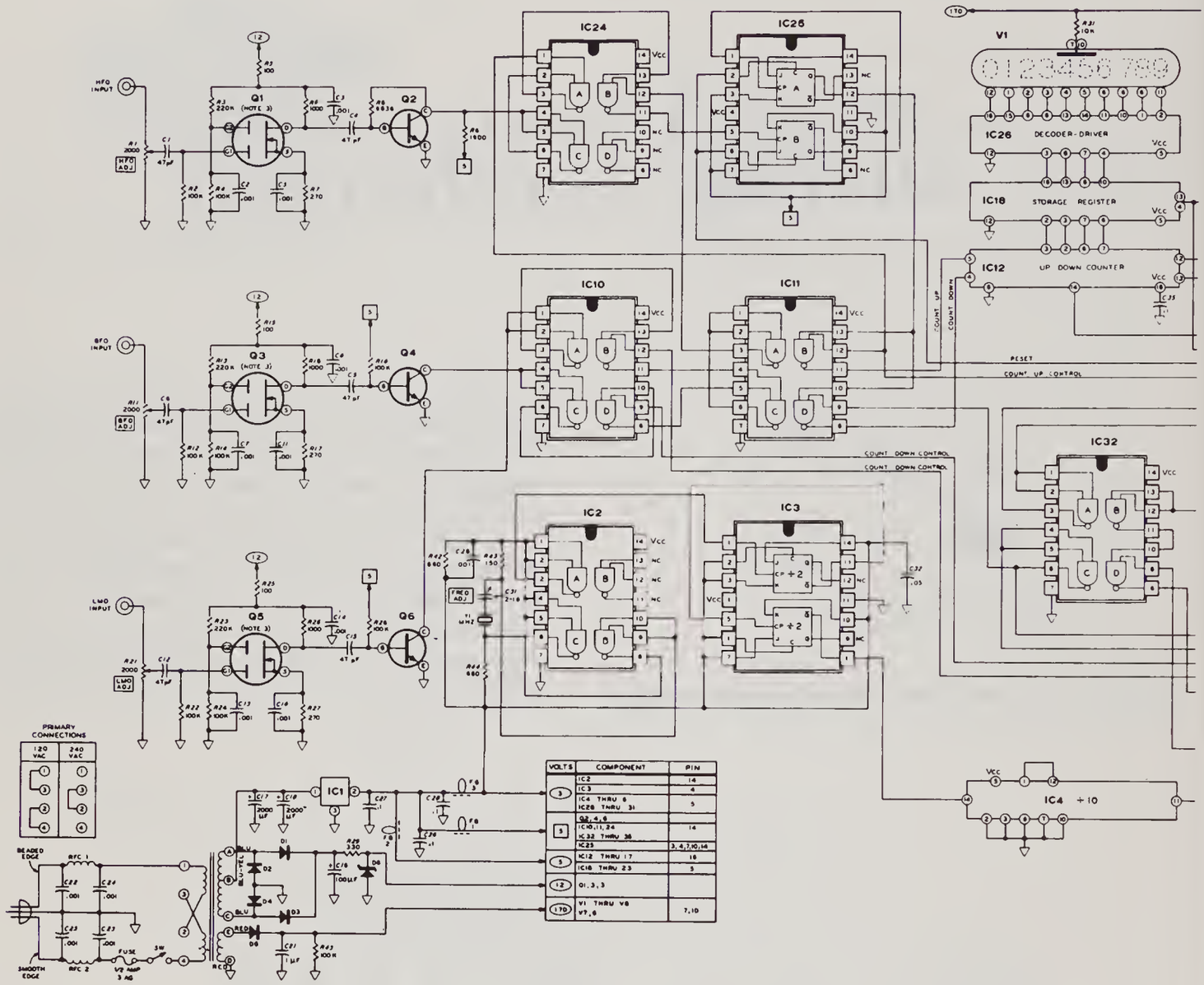
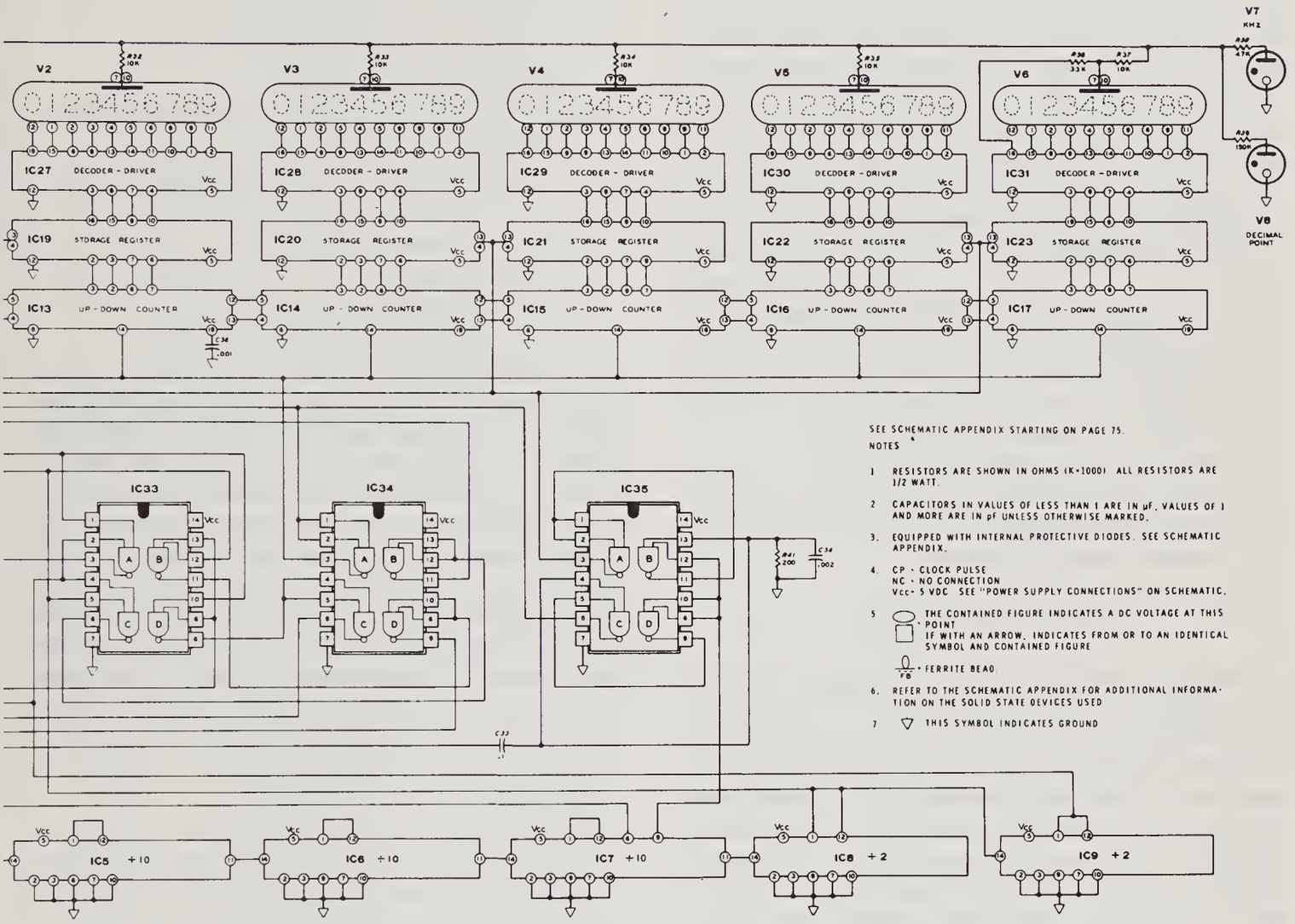


Fig. 7-3. Schematic diagram of



SEE SCHEMATIC APPENDIX STARTING ON PAGE 75.

NOTES

1. RESISTORS ARE SHOWN IN OHMS (K=1000) ALL RESISTORS ARE 1/2 WATT.
2. CAPACITORS IN VALUES OF LESS THAN 1 ARE IN μF, VALUES OF 1 AND MORE ARE IN pF UNLESS OTHERWISE MARKED.
3. EQUIPPED WITH INTERNAL PROTECTIVE DIODES. SEE SCHEMATIC APPENDIX.
4. CP - CLOCK PULSE
   NC - NO CONNECTION
   Vcc - 5 VDC SEE "POWER SUPPLY CONNECTIONS" ON SCHEMATIC.
5. THE CONTAINED FIGURE INDICATES A DC VOLTAGE AT THIS POINT
   IF WITH AN ARROW, INDICATES FROM OR TO AN IDENTICAL SYMBOL AND CONTAINED FIGURE
   FB - FERRITE BEAD.
6. REFER TO THE SCHEMATIC APPENDIX FOR ADDITIONAL INFORMATION ON THE SOLID STATE DEVICES USED
7. ▽ THIS SYMBOL INDICATES GROUND

SCHEMATIC OF THE HEATHKIT®

DIGITAL FREQUENCY DISPLAY

MODEL SB-650

Courtesy, Heath Co.

the digital frequency display unit.

utilized to calculate and process the operating frequencies from three oscillators in the receiver—the high-frequency oscillator, the linear master oscillator, and the beat-frequency oscillator. The result of this processing is the operating frequency, which in turn is displayed in kilohertz units. Typical trouble symptoms that may be encountered in this type of digital equipment are:

1. Display tubes and lamps dark.
2. Display tubes dark; lamps glowing normally.
3. Readout "stuck-at" 00 000.0.
4. Some display tubes showing incorrect readout.
5. One display tube "stuck-at" a particular numeral.
6. More than one digit glowing in a single display tube.
7. Readout "stuck-at" 99 999.9.
8. Blurred and unreadable display.
9. Erratic operation.
10. Random readout that changes only when power switch is thrown.

GENERAL DISCUSSION

Troubleshooting a digital frequency display unit requires an understanding of its functions. In this discussion, circuit actions are explained with reference to the block diagram in Fig. 7-2 and the schematic diagram in Fig. 7-3. The three inputs are energized by signals from the three oscillators in a companion amateur radio receiver or in a 5-band transceiver operating below 30 MHz. An up/down counter is used to count up the hfo (high-frequency oscillator) frequency, and then to count down and thereby to subtract the frequencies of the lmo (linear master oscillator) and the bfo (beat-frequency oscillator). In turn, the operating frequency is calculated and is displayed in kilohertz units by six illuminated tubes. For example, an operating frequency calculation in the 80-meter band is made as follows:

High-frequency oscillator (count up)	12 395.0 kHz
Linear master oscillator (count down)	−5 199.5
	7 195.5
Beat-frequency oscillator (count down)	−3 393.6
Operating frequency (display)	3 801.9

Counting occurs in cycles, and the displayed frequency is recalculated once each 160 milliseconds, or approximately six times per second. As will be discussed subsequently, each 160-ms cycle is subdivided into four parts of 40 ms each. Three of these intervals are used in counting procedures, and the fourth interval is used to process and display the count. Observe the input circuitry shown in Fig. 7-4. Except for the bias on transistor Q2, each of the three input circuits is identical; the output is connected to a different gate in each case, as shown in Fig. 7-3. The following explanation is for the hfo (high-frequency oscillator) input circuit.

With reference to Fig. 7-4, control R1 adjusts the level of the input signal to Q1. This transistor is a MOSFET that provides a high input impedance to avoid objectionable loading of the signal source. Other resistors and capacitors con-

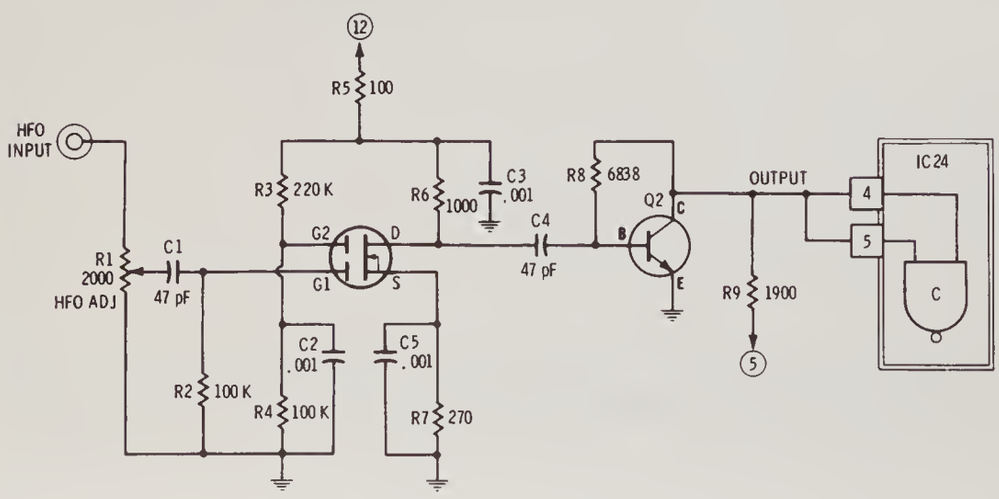


Fig. 7-4. Input circuitry of digital frequency display unit.

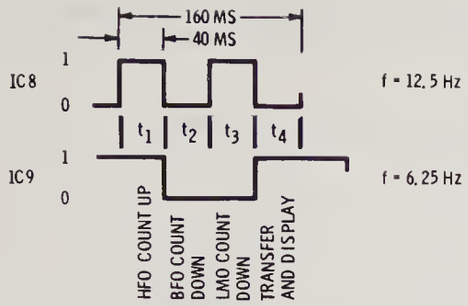


Fig. 7-5. Relationships of output waveforms of IC8 and IC9.

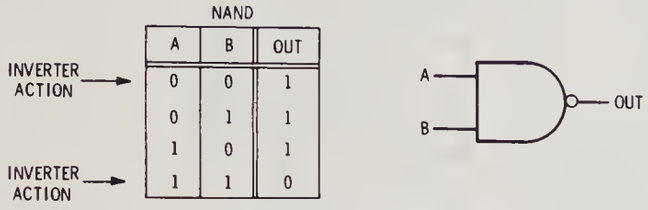


Fig. 7-6. NAND gate and truth table.

nected to Q1 are the usual biasing, bypass, and load components. Transistor Q1 amplifies the input signal, and transistor Q2 functions as a buffer for the digital logic load. Components R8 and R9 are bias resistors for Q2. With reference to Fig. 7-3, the clock oscillator is made up of IC2, the 1-MHz crystal Y1, and associated components. Crystal Y1 is adjusted to precise frequency by trimmer capacitor C31. Note that the 1-MHz output frequency from IC2 is divided by the clock-frequency divider (IC3 through IC9) as follows:

	Function	*Output*
IC3	Divide by 4	250 kHz
IC4	Divide by 10	25 kHz
IC5	Divide by 10	2.5 kHz
IC6	Divide by 10	250 Hz
IC7	Divide by 10	25 Hz
IC8	Divide by 2	12.5 Hz
IC9	Divide by 2	6.25 Hz

Observe in Fig. 7-3 that the four outputs from the clock-frequency divider come from IC7, IC8, and IC9. These clock-frequency outputs provide the timing sequence for the system. Next, Fig. 7-5 shows the relationships between the output waveforms of IC8 and IC9 during one cycle of IC9 operation. This cycle is 160 ms in duration (1 sec/6.25 Hz). Thus, the four periods are each 40 ms in duration; they are designated as t_1, t_2, t_3, and t_4. Functions occurring during each of these periods are indicated in Fig. 7-5. Only NAND gates are employed in the logic system. A NAND gate can be used as an inverter by applying a logic-high level or a logic-low level to both inputs, as stated by the truth table in Fig. 7-6.

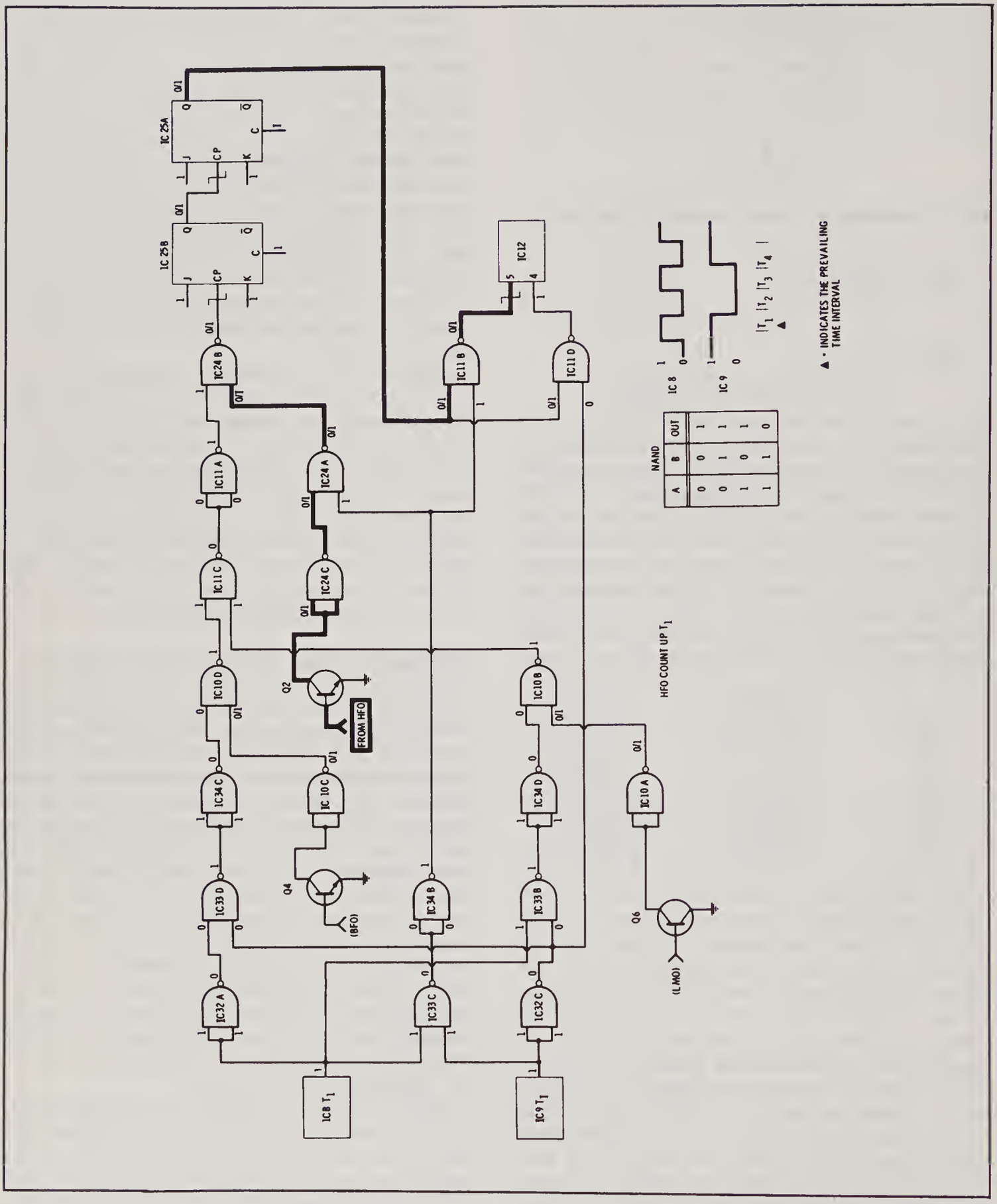
At this point, it is helpful to briefly review NAND-gate action. Logic-high corresponds to a 1 level, and logic-low corresponds to a 0 level. If a NAND gate has a logic 0 at any input, the output will always be a logic 1. A logic 0 at any input inhibits (closes) the gate, since the output will always remain high, regardless of the logic level applied at the other input. Conversely, if one input to a NAND gate is held high, the gate is open because changing the logic level at the other input will change the logic level at the output. Observe also that the truth table states that the logic level of the output is the complement (the output signal is inverted) of the input logic level when both inputs are the same.

Logic levels are indicated at the inputs and outputs of most of the gates in the following diagrams. Levels are indicated as either 1 or 0. If a level is shown as 0/1, it means that the logic level is changing back and forth at the signal frequency. Note also that the symbol ⌐_ crossing the input line to an IC means that the IC will toggle, or change state, when the trailing edge of the input waveform is applied, whereas the symbol _⌐ means that the IC will toggle when the leading edge of the input waveform is applied.

SEQUENCER AND MULTIPLEXER CIRCUITRY

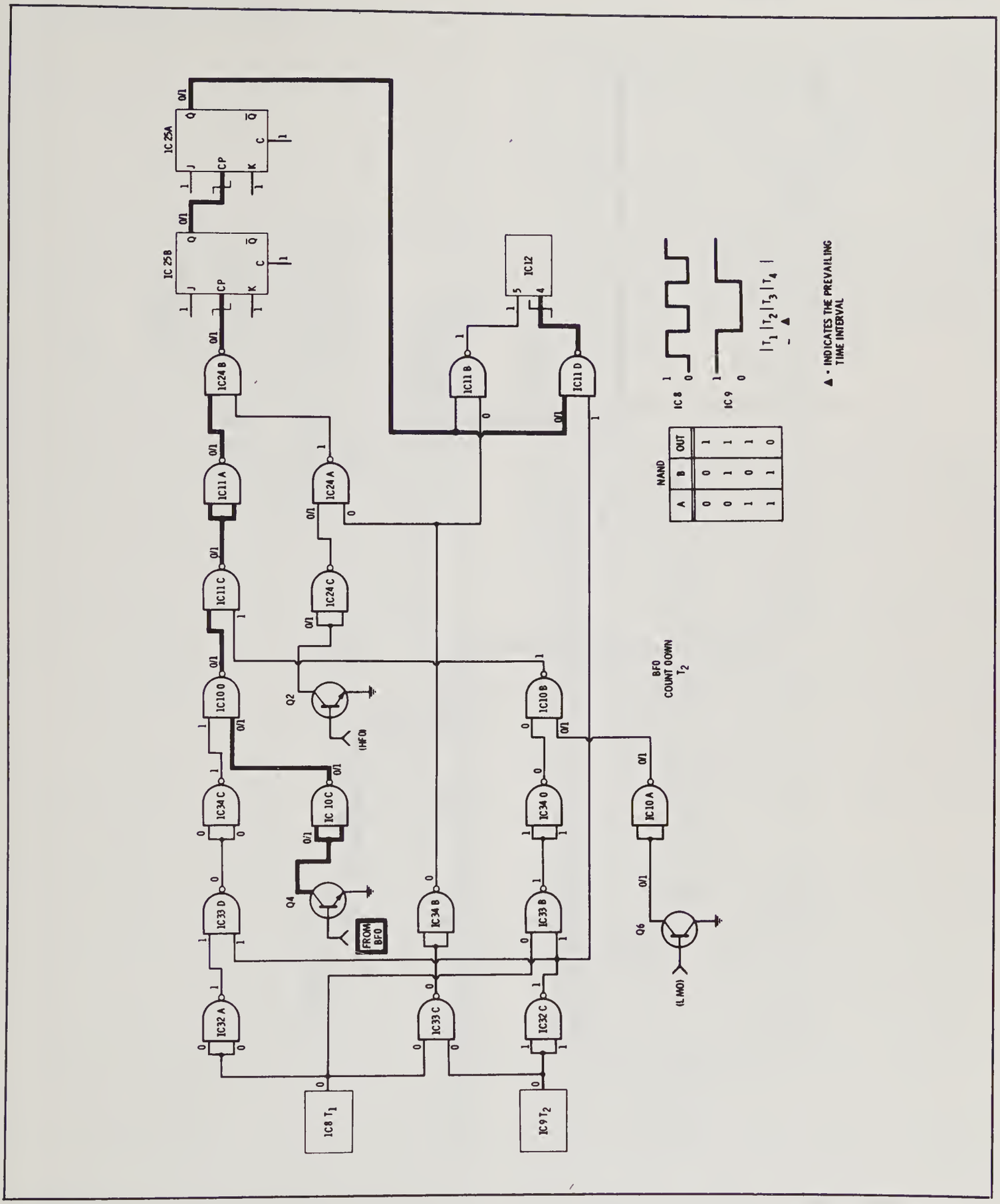
The sequencer and multiplexer circuits have the function of processing the output logic from the clock-frequency divider so that the three input signals are selected in correct sequence and routed through the proper channels to the up/down counters. Transistors Q2, Q4, and Q6 function as interfaces to change the analog inputs into digital-logic voltage levels. In each case, the gate following the transistor operates as a wave shaper. Note that an interface is a junction between systems or subsystems that provides compatibility between the different functions. In this example, the interface changes the analog input signal into discontinuous (discrete) logic voltage levels. Thus, although a sine wave has a continually changing value, the interface has only logic-high or logic-low outputs.

Observe that the arrangements shown in Figs. 7-7, 7-8, and 7-9 are similar, except that they differ with respect to signal sources, signal paths, and the control logic from the outputs of IC8 and IC9. Note that the signal source is shown as a box in each diagram and that the signal path is shown



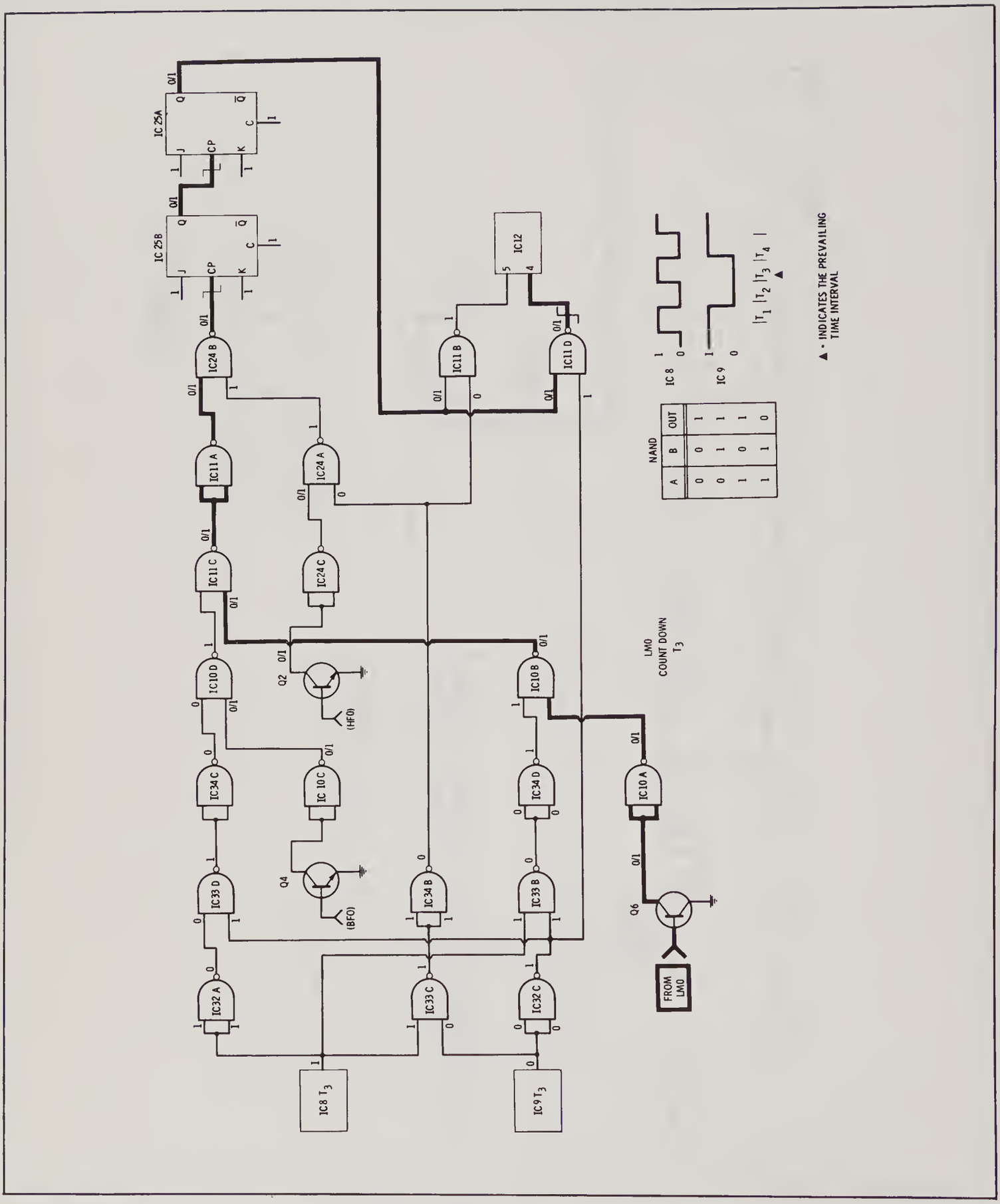
Courtesy, Heath Co.

Fig. 7-7. The hfo input arrangement.



Courtesy, Heath Co.

Fig. 7-8. The bfo input arrangement.



Courtesy, Heath Co.

Fig. 7-9. The lmo input arrangement.

in heavy lines from the source to the input of the up/down counter, IC12. Pin 5 of IC12 is the count-up terminal, and pin 4 is the count-down terminal. Each of the diagrams shows the particular waveform relationship of IC8 and IC9 for the function illustrated. The three oscillator inputs are present continuously. However, all three are inhibited by gates during the t_4 time period. Only the proper signal is permitted to enter during the other three time periods. Fig. 7-10 shows the logic levels during time period t_4 when there is no counting process.

Because the up/down counter has a high-frequency limitation, IC25 provides a divide-by-four action to bring the 10-meter band hfo signals within the operating frequency range of the counter. With reference to Fig. 7-7, during the time that the hfo input is being counted, the logic levels of time period t_1 apply and the count-up operation proceeds. Note that the signal input is through Q2 and along the heavy lines to pin 5 of IC12, the count-up input terminal. As shown in the truth table, the logic levels from the outputs of IC8 and IC9 control the gates so that only the signal from the hfo input is counted.

Observe that the signal from the bfo input (Q4) is blocked from entering the counter because IC10D is inhibited by a logic-low level at one of its inputs. Similarly, the lmo signal (Q6) is blocked from entering the counter because IC10B is inhibited by a logic-low level at one of its inputs. At the same time, the hfo signal can be processed because one input of IC24A is held to a logic-high level by IC34B and the output IC24A then alternates at the frequency of the signal at its other input. Note that gate IC24B is open because one of its inputs is held logic-high by IC11A. The flip-flops are conventional. They are connected so that a negative-going signal at the flip-flop input will cause a change in the logic level of the outputs. On the other hand, a positive-going signal has no effect. Thus, each flip-flop divides its input frequency by 2, as depicted in Fig. 7-11.

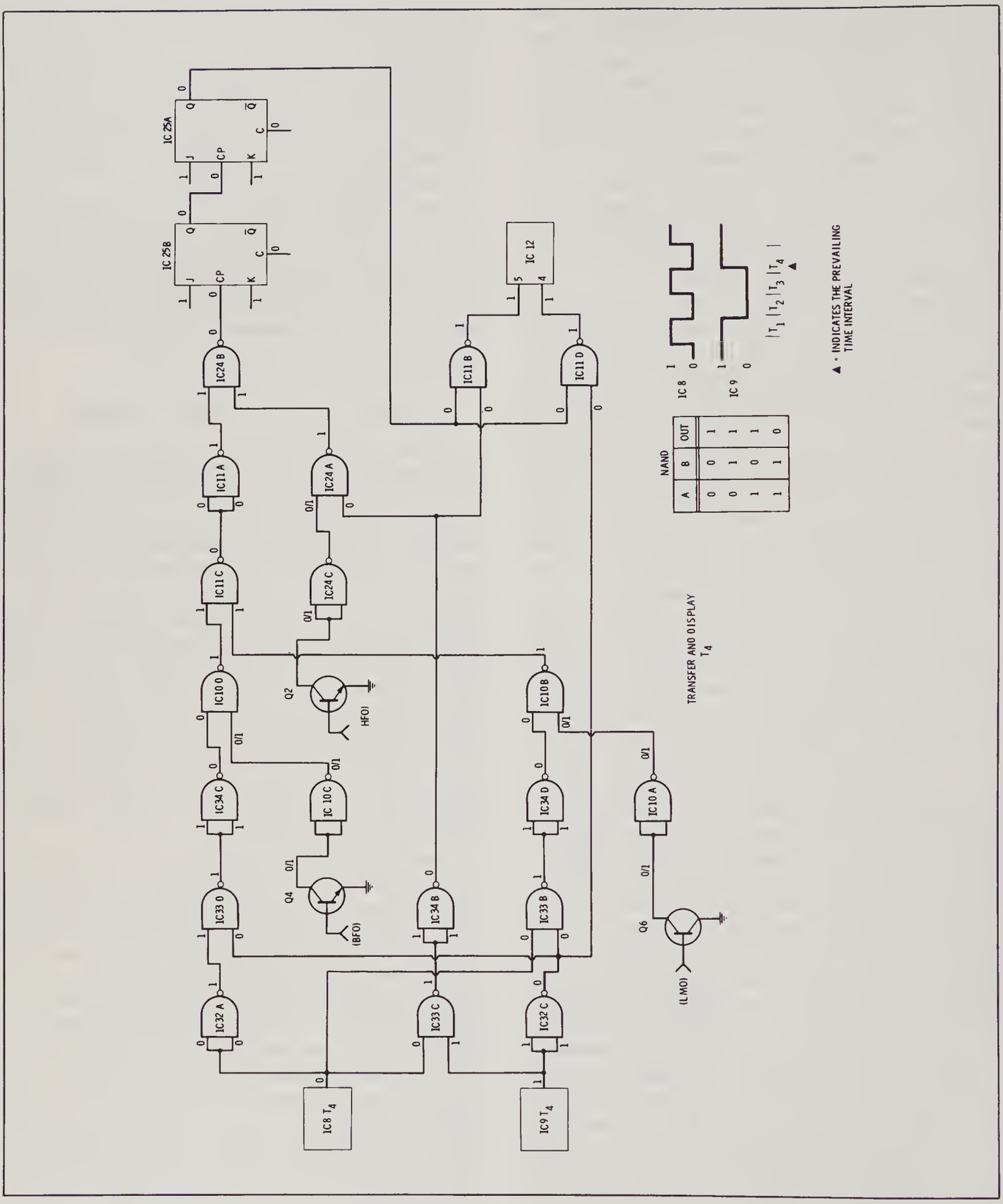
Since IC25 contains two flip-flops, it performs a divide-by-four function. Note that the signal path is then through IC11B (inasmuch as one input is held logic-high by IC34B) and thence to pin 5 of IC12. The signal is prevented from passing through IC11D because it is inhibited by the logic-low from IC32C. Next, consider the bfo input arrangement depicted in Fig. 7-8. The bfo input is selected by logic levels of IC8 and IC9 during the time interval, t_2. Note that the signal path is through Q4 and along the heavy lines to IC25. Gate IC24A, which is in the hfo signal path, is now inhibited by a logic-low at one of its inputs; IC10B in the lmo signal path is similarly inhibited. Observe that the signal path from IC25 is through IC11D to pin 4 of IC12, which is the count-down input of the counter.

Next, consider the lmo input arrangement shown in Fig. 7-9. During time interval t_3, IC8 and IC9 enable the signal path from Q6 and inhibit gates IC24A and IC10D in the signal paths from Q2 and Q4. As was previously explained for the bfo input arrangement, the lmo signal proceeds through IC11D to pin 4 of IC12.

TRANSFER AND STORAGE ACTIONS

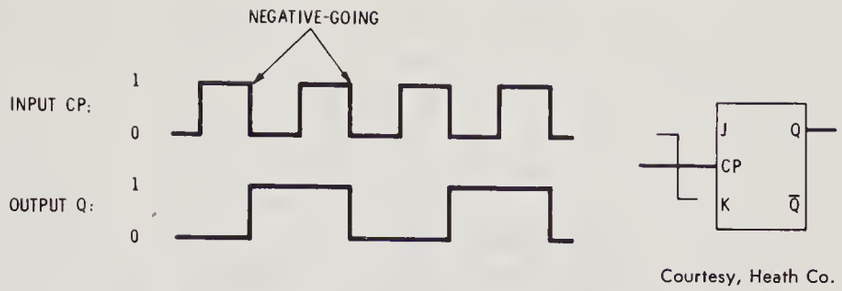
During time interval t_4, the IC8 and IC9 output logic causes gates IC24A, IC10B, and IC10D to be inhibited as shown in Fig. 7-10. This inhibition prevents the three oscillator signals from reaching the up/down counter. Note that the logic output at pin 8 of IC7 changes midway during the t_4 interval to divide the interval into two 20-ms periods. Thus, the output is high during the first period and is low during the second period (see Figs. 7-12 and 7-13). Fig. 7-12 depicts generation of the transfer pulse for the storage registers of the up/down counter during the first 20 ms of time period t_4. Note that pin 8 of IC7 is high and holds gate IC35B open. In turn, the outputs from IC8 and IC9, through a series of gates, apply a logic-high level to one input of IC32D, thereby holding that gate open.

Note also that two cycles of a square wave from pin 9 of IC7 are applied to one input of IC32D. These square waves appear at the gate output and are then differentiated by C33 and R41 to form a positive-going pulse at the input of IC35B. While gate IC35B is held open, the input is inverted and a negative-going pulse appears at the gate output. This pulse becomes inverted by gate IC35A to produce a positive pulse which is fed to storage registers IC18 through IC23. The pulse commands the transfer of the count from the up/down counter to the storage registers. This topic is explained in greater detail subsequently. Fig. 7-13 shows how the clear pulses are derived for the up/down counters and for IC25. In turn, these pulses return the counters and the flip-flop to the 0-output state for the next count.



Courtesy, Heath Co.

Fig. 7-10. Transfer-and-display function.



Courtesy, Heath Co.

Fig. 7-11. Input-signal frequency is divided by 2.

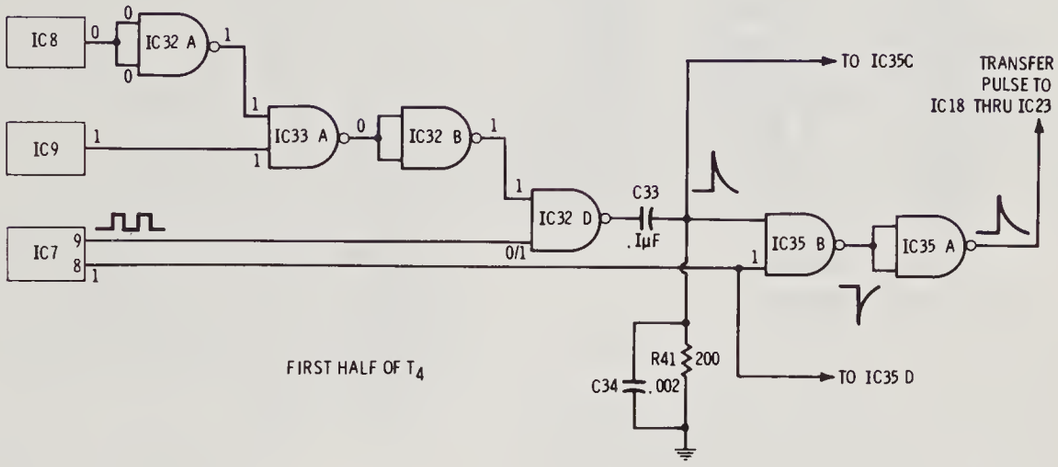


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Fig. 7-12. Conduction during the first half of time period t_4.

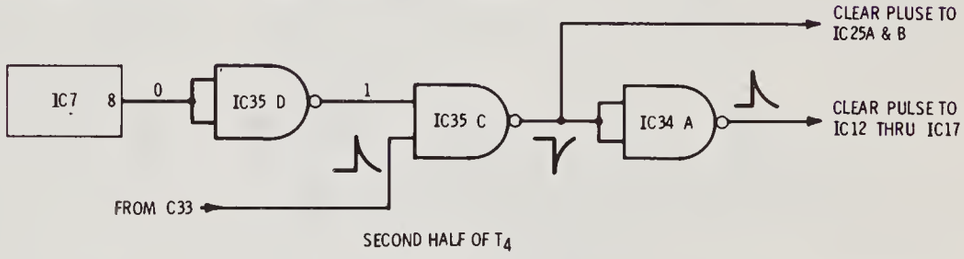

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Fig. 7-13. Conduction during the second half of time period t_4.

During the second half of the t_4 interval, pin 8 of IC7 is logic-low. Note that the inversion of the IC35D output to a high level holds IC35C open so that it passes and inverts the pulse from C33, as shown in Fig. 7-13. This negative-going pulse from IC35C is utilized as the clear pulse for IC25, whose Q outputs are accordingly returned to the 0 state in preparation for the succeeding counting cycle. Observe that the negative pulse from IC35C is inverted by IC34A to a positive pulse, which is used as the clear pulse to return the up/down counters IC12 through IC17 to zero.

COUNTING AND DISPLAY

At the beginning of time interval t_4, which is the transfer-and-storage period, the up/down count has been completed and is being held in the storage-registers. This count is in bcd (binary-coded decimal) units, or bits (binary digits). Each up/down counter has a 4-bit bcd output. The inputs to the storage registers are opened for a few microseconds during time period t_4 by a transfer pulse. This allows the state of the completed binary count to be transferred to the storage register, which in turn holds the count until it receives another transfer pulse following completion of the next count. The chief reason for employing a storage register is that the display is held steady until the following count has been completed. If this register were not utilized, a blur of changing numbers would occur during each count, and the display would remain stationary for only a small fraction of a second. Note that the count held by the storage registers appears at the input of the decoder/driver, which decodes the binary count

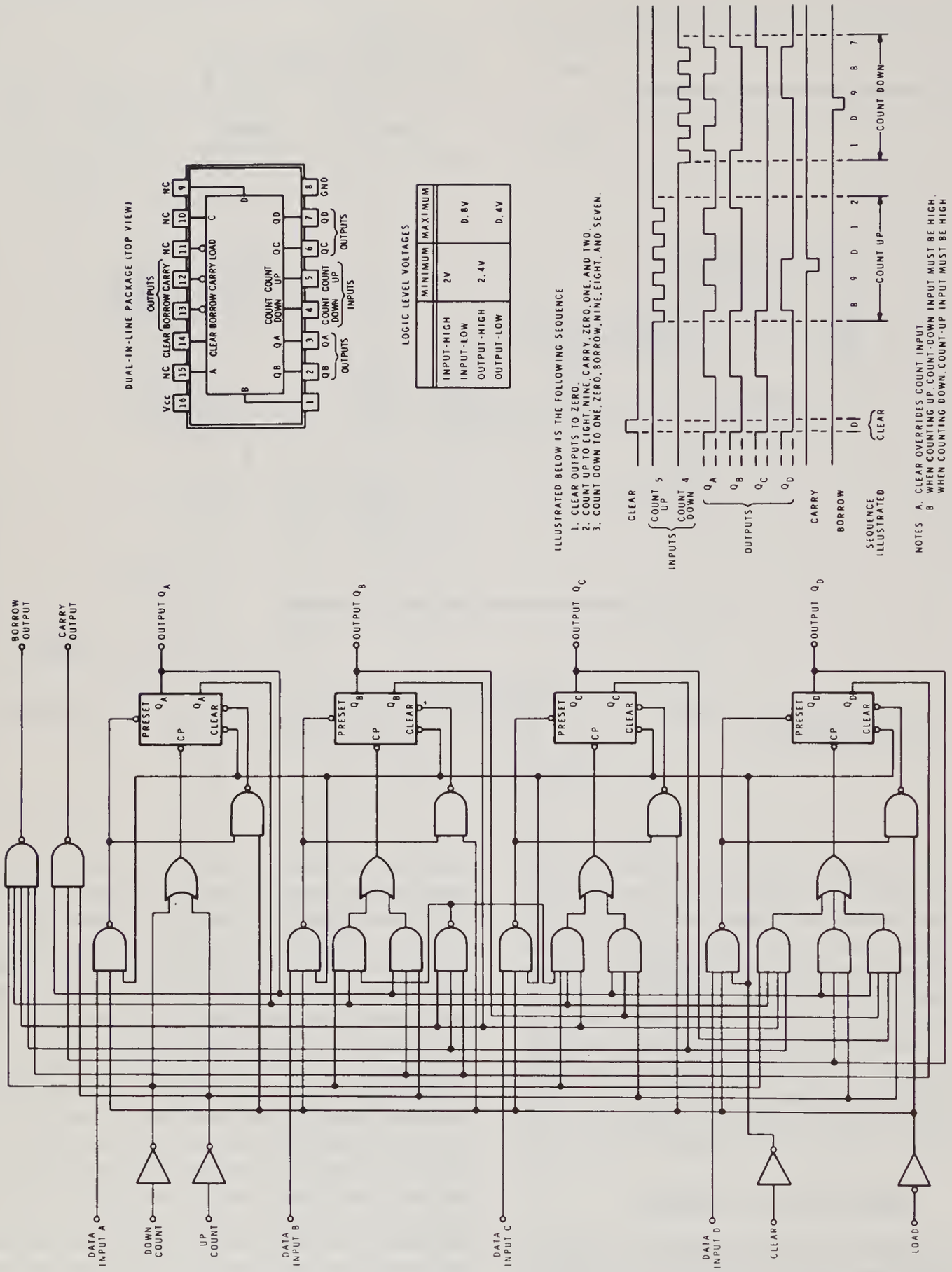


Fig. 7-14. Up/down counter block diagram and operating sequence.

and turns on the corresponding decimal number in the display tube.

UP/DOWN COUNTER OPERATION

The counters employed in the aforementioned system are called synchronous 4-bit up/down counters. Each counter is contained in a dual in-line IC package and has four outputs in the 1, 2, 4, 8 binary notation, as explained previously. Fig. 7-14 shows a block diagram of the counter, a partial waveform timing chart, and a table depicting the voltage levels which the device recognizes as a logic-high or logic-low. Observe in the waveform chart that the outputs change state when either input makes the transition from logic-low to logic-high. Pin 5 is the count-up input terminal, and pin 4 is the count-down input terminal. Note that the direction of counting (up or down) is determined by the input to which the signal is fed while the other count input is held logic-high.

STORAGE REGISTERS

Observe that the four binary outputs of an up/down counter are always present at the four inputs of a storage register, which is actually a 4-bit latch. In turn, the information that is present at each latch input will be transferred to its Q output whenever the clock input is logic-high. Note that the output level of the storage register will follow the input as long as the clock input is high. On the other hand, when the clock input goes low, the state of the Q output is retained until the clock input again goes high. Accordingly, when the positive-going transfer pulse arrives at the clock inputs from IC35A (Fig. 7-12), the storage-register inputs are opened momentarily. During this brief interval, the output states of the counter are transferred to the storage register where they are retained at the Q outputs until the next transfer pulse arrives.

DECODER/DRIVERS

The decoder/drivers receive the binary count present at the Q outputs of the storage registers and decode the binary count so that one of the ten decoder/driver outputs is grounded. This results in displaying (illuminating) the corresponding decimal number in a display tube. The truth table in Fig. 7-15 gives the information necessary

NOTE:
THESE ARE THE DISPLAY TUBE NUMBERS WHICH WILL BE TURNED ON BY THE 1D DECODER-DRIVER OUTPUTS. THE ACTIVATED OUTPUT WILL BE "LOW" AND THE OTHER NINE OUTPUTS "HIGH". FOR EXAMPLE, IF THE NUMBER "7" IS ILLUMINATED IN THE DISPLAY TUBE, PIN 1D OF THE DECODER-DRIVER WILL BE "LOW" AND THE OTHER NINE OUTPUT PINS WILL BE "HIGH"

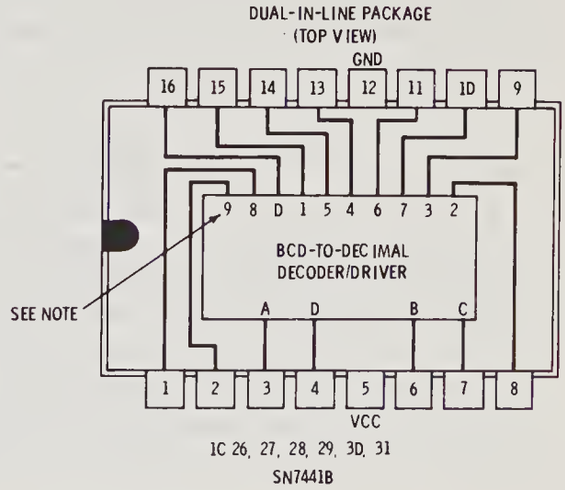
LOGIC LEVEL VOLTAGES

	MINIMUM	MAXIMUM
INPUT-HIGH	2 V	
INPUT-LOW		0.8 V
OUTPUT-HIGH	2.5 V	90.0 V

Fig. 7-15. Truth table and terminal arrangement for decoder-driver.

THRUTH TABLE

INPUTS				OUTPUT ON*
D	C	B	A	
0	0	0	D	D
0	0	0	1	1
D	0	1	0	2
0	0	1	1	3
D	1	0	D	4
D	1	D	1	5
0	1	1	0	6
D	1	1	1	7
1	D	D	0	8
1	D	0	1	9



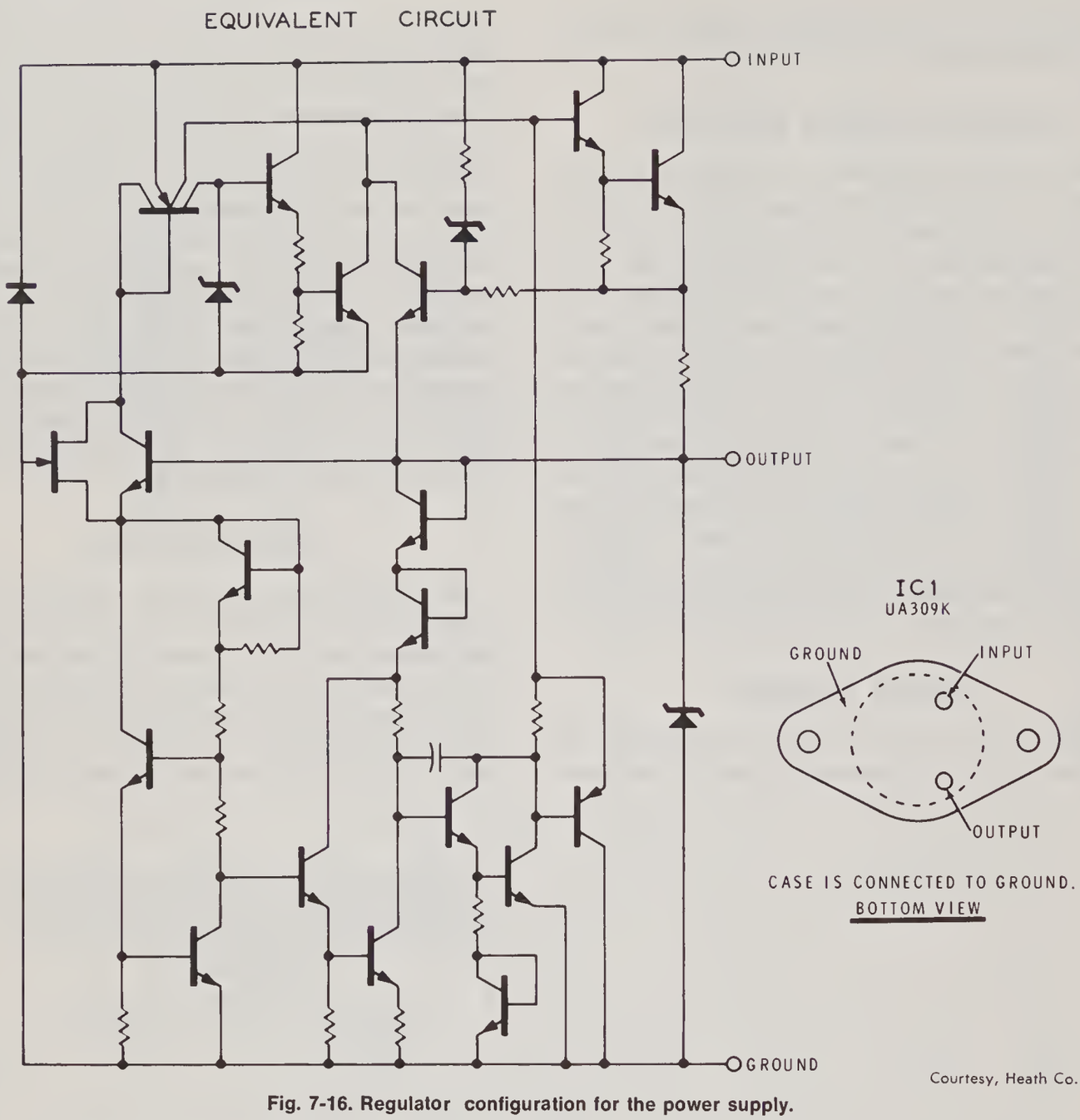


Fig. 7-16. Regulator configuration for the power supply.

to relate the binary input levels to the output logic levels employed to turn on the proper number in the display tube.

DISPLAY TUBES

Note in Fig. 7-3 that the anode (pins 7 and 10) of each display tube is connected to the 170-volt dc supply line through a 10K current-limiting resistor. The decimal-point connections on each socket (pins 13 and 14) are not used. Each of the remaining ten pins is connected to a separate cathode of the tube; as explained previously, each cathode is shaped in the form of a decimal number from 0 through 9. Whenever one of these cathodes is grounded (held logic-low) by the decoder/driver, the gas in front of the cathode ionizes and the cathode glows. Of course, the cathodes that are held logic-high by the decoder/driver outputs will not glow. Neon tubes V7 and V8 illuminate the kilohertz indication and the decimal point. These neon tubes are turned on and off at the same time as the display tubes.

A regulated output from the power supply is obtained by a voltage-regulating circuit contained in IC1. Fig. 7-16 shows the configuration of this IC. It provides a regulated 5 volts dc for the digital circuits and for transistors Q2, Q4, and

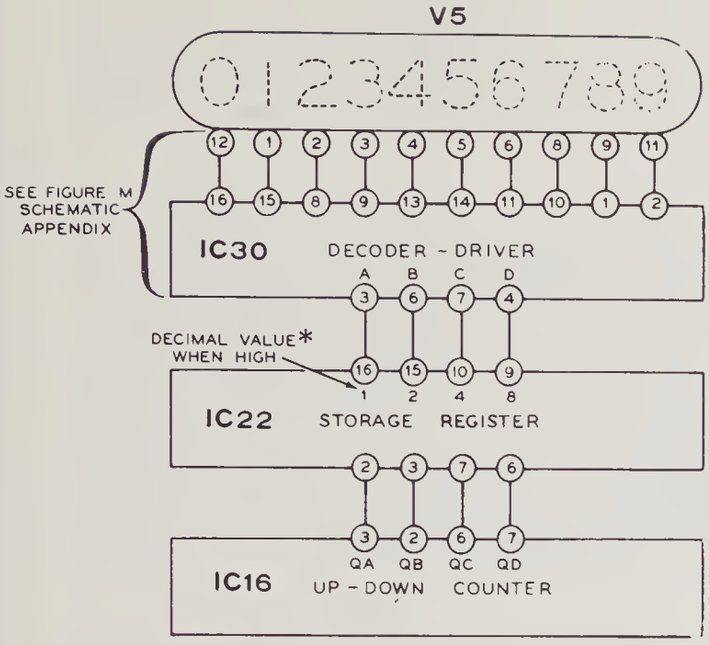


Figure 5-2

*Add the values of the highs to determine the decimal equivalent. For example, if pins 16 and 10 of IC22 are high (pins 15 and 9 remain low), then the decimal equivalent is 5 (1+4=5). If only pin 9 is high, the decimal equivalent is 8. If all pins are low, the decimal equivalent is 0.

Courtesy, Heath Co.

Fig. 7-17. Counting and display circuits.

BCD COUNT SEQUENCE (SEE NOTE)

COUNT	OUTPUT			
	D	C	B	A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

(A) Count sequence.

LOGIC LEVEL VOLTAGES

	MINIMUM	MAXIMUM
INPUT-HIGH	2 V	
INPUT-LOW		0.8 V
OUTPUT-HIGH	2.4 V	
OUTPUT-LOW		0.4 V

(B) Logic-level voltages.

Fig. 7-18. Bcd count sequence and logic-level voltages.

Q6. Three ferrite beads and capacitors C26, C27, and C28 on the three 5-volt output lines function to suppress vhf transients.

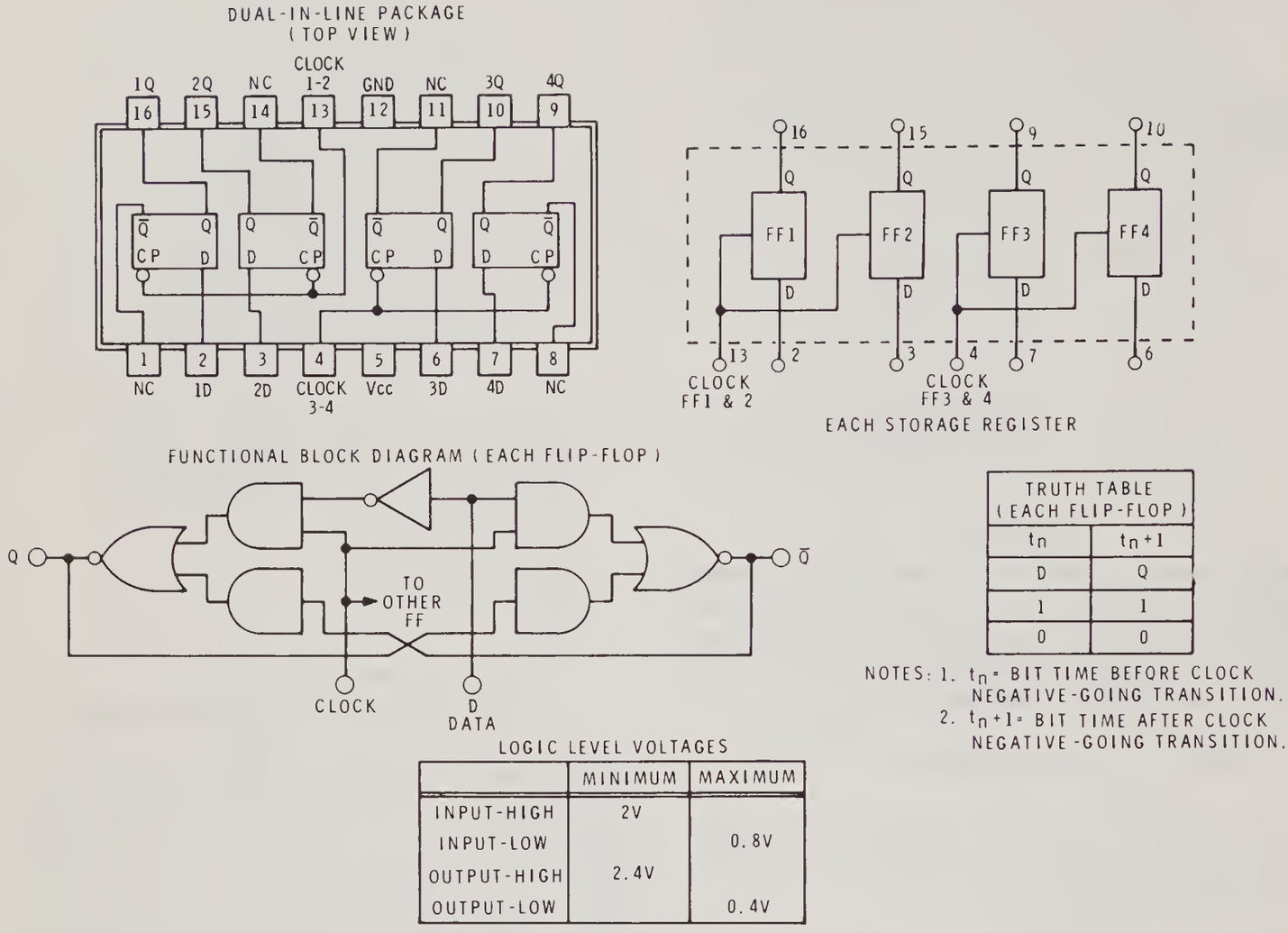
TROUBLESHOOTING TECHNIQUES

Each IC should be pressed firmly into its socket to ensure good contacts. Note that in this example, ICs 12 through 17 can be interchanged. In case one display tube shows two numerals simultaneously, interchange it with one of the other display tubes to determine if the tube or the circuit is faulty. If the circuit is defective and there is no short circuit between circuit-board conductors, the associated decoder/driver IC should be interchanged with one of the others. This technique is also useful in other single-digit trouble situations, and can be extended to interchanging the storage register and up/down counter ICs.

Consider the counting and display arrangement depicted in Fig. 7-17. It consists of the up/down counter and the associated storage register, decoder/driver, and display tube. A transistor voltmeter (tvm) can be employed to check the logic states of the storage registers, decoder/drivers, and display tubes. A logic-high level for these devices is 2.4 volts, or more, whereas a logic-low level is 0.4 volt or less. The up/down counters cannot be accurately checked with a voltmeter because their outputs change rapidly with the count. However, the substitution method just explained above is a practical way to check their condition.

With reference to Fig. 7-17, if tube V5 displays a "5" when a "3" should be seen (80-meter band), IC16 may be transposed with one of the other up/down counters that shows a correct display. Then, if V5 still displays a "5," it may be concluded that the up/down-counter IC is operational. On the other hand, if the display changes to a "3," the IC is probably defective. In this case, it is advisable to reinsert the original IC into its socket to make certain. Fig. 7-18 gives the bcd count sequence and shows the pertinent logic-level voltages.

Continuing this procedure, if the display remains a "5," check the outputs of storage register IC22 (see Fig. 7-19). If pins 16 and 15 are logic-high, and pins 10 and 9 are logic-low, it may be concluded that the storage register is normal (1 + 2 = 3). Next, the decoder/driver, IC30, should have pin 9 logic-low to turn on the 3 in the display



Courtesy, Heath Co.

Fig. 7-19. Storage-register data.

tube, and all other output pins should be logic-high. In case pin 9 should be logic-low, but a 5 is displayed, then the defect is probably in the tube and it should be substituted with one of the other display tubes for a cross-check. Finally, if the previous tests are all indicative of a "5," then it is logical to assume that the trouble is occurring ahead of the counting and display circuits.

1. Display Tubes and Lamps Dark

Possible causes of dark display tubes and lamps are:

a. Power-supply voltage subnormal or zero.
b. Blown fuse (correct the cause before replacing).
c. Short circuit along 5-, 12-, or 170-volt line.
d. Check diode D5 in power supply (Fig. 7-3).
e. Defective power transformer (not likely, but possible).

2. Display Tubes Dark; Lamps Glow Normally

Common causes of dark display tubes, with kilohertz and decimal lamps continuing to glow, are:

a. Defective IC1 (Fig. 7-16).
b. Open or shorted rectifier diode: D1, D2, D3, or D4 (Fig. 7-3).
c. Short circuit along 5-volt line.

3. Readout "Stuck-at" 00 000.0

Probable causes of a "stuck-at" zero readout are:

a. Dead 12-volt supply line.
b. Clock stopped; meter pointer should oscillate on ▲ voltages for IC8 and IC9 when clock is running (see Fig. 7-20).
c. Defective clock crystal.
d. Faulty IC2, 10, 11, 24, 32, 33, 34, or 35 (see Fig. 7-21).
e. Defective divider flip-flop (IC3 through 9).
f. Defect in IC25 (see Fig. 7-22).
g. IC2 reversed in its socket; display is locked in.

4. Some Display Tubes Showing Incorrect Readout

When some display tubes, but not all, show incorrect readouts, preliminary suspicion falls on the associated readout circuitry. Check display tubes and connections, decoder/driver, storage register, and up/down counter ICs.

5. One Display Tube "Stuck-at" a Particular Numeral

If one digit is locked on a numeral and will not follow the lmo tuning, suspicion falls on the readout circuitry. Check the decoder/driver, storage register, and up/down counter ICs.

6. More Than One Digit Glowing in a Single Display Tube

When this trouble symptom is encountered, the following possible causes should be checked:

a. Short circuit between circuit-board conductors.
b. Defective decoder/driver IC associated with the display tube.
c. Bent or broken pin on readout tube.
d. Deteriorated display tube.

7. Readout "Stuck-at" 99 999.9

This "stuck-at" trouble symptom indicates a defect in IC25 (Fig. 7-22).

8. Display Blurred and Unreadable

A blurred and unreadable display is most likely to be caused by a defect in IC35 (Fig. 7-21).

9. Erratic Operation

This trouble symptom indicates a defect in IC12, IC24, or IC25 (Fig. 7-3).

10. Random Readout That Changes Only When Power Switch Is Thrown

Probable causes for this trouble symptom are:

a. Defective IC32 or IC33 (Fig. 7-3).
b. Clock not running.
c. IC2 reversed in socket.
d. Defective clock crystal.
e. Defect in IC2 through IC9 (Fig. 7-3).

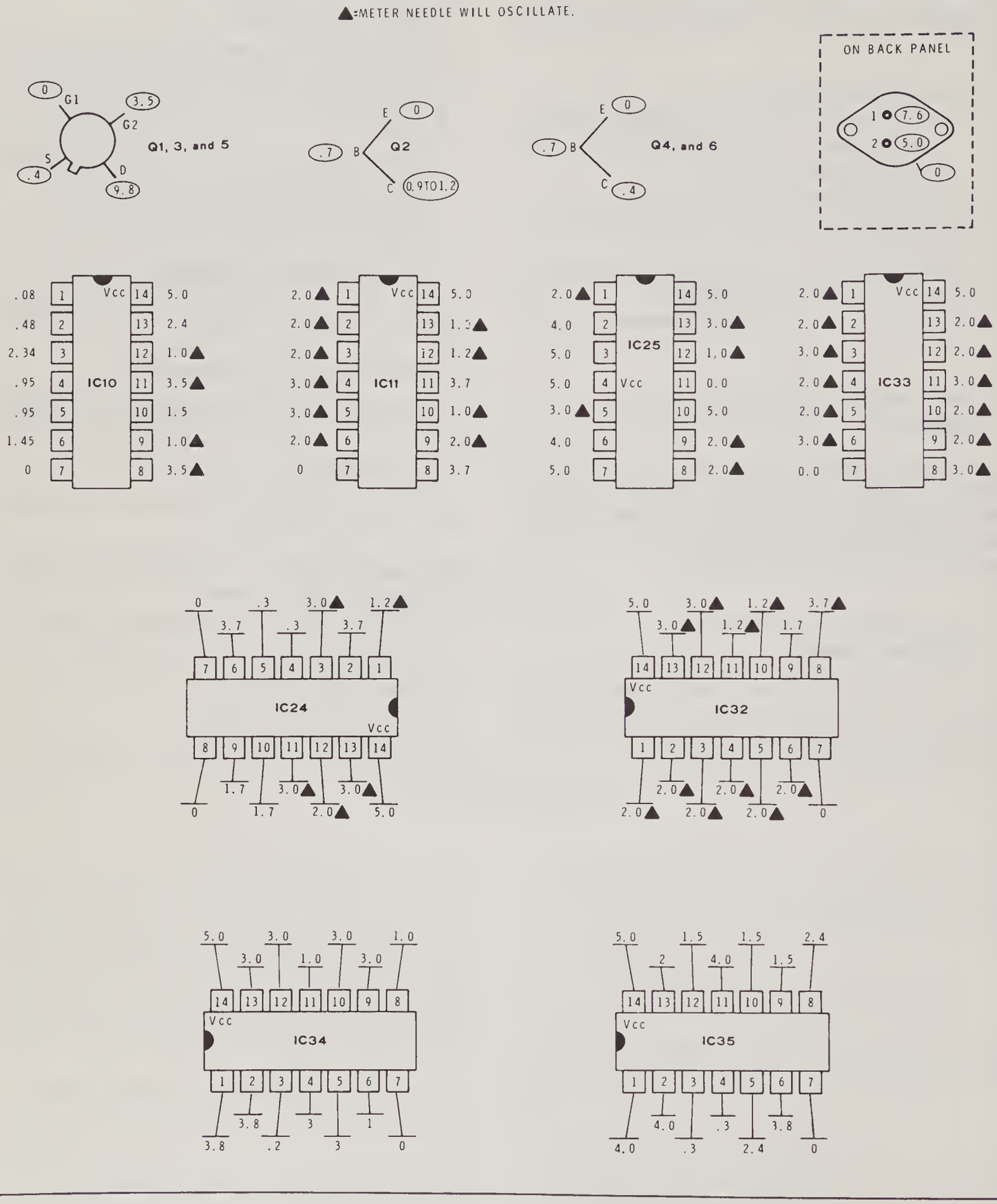
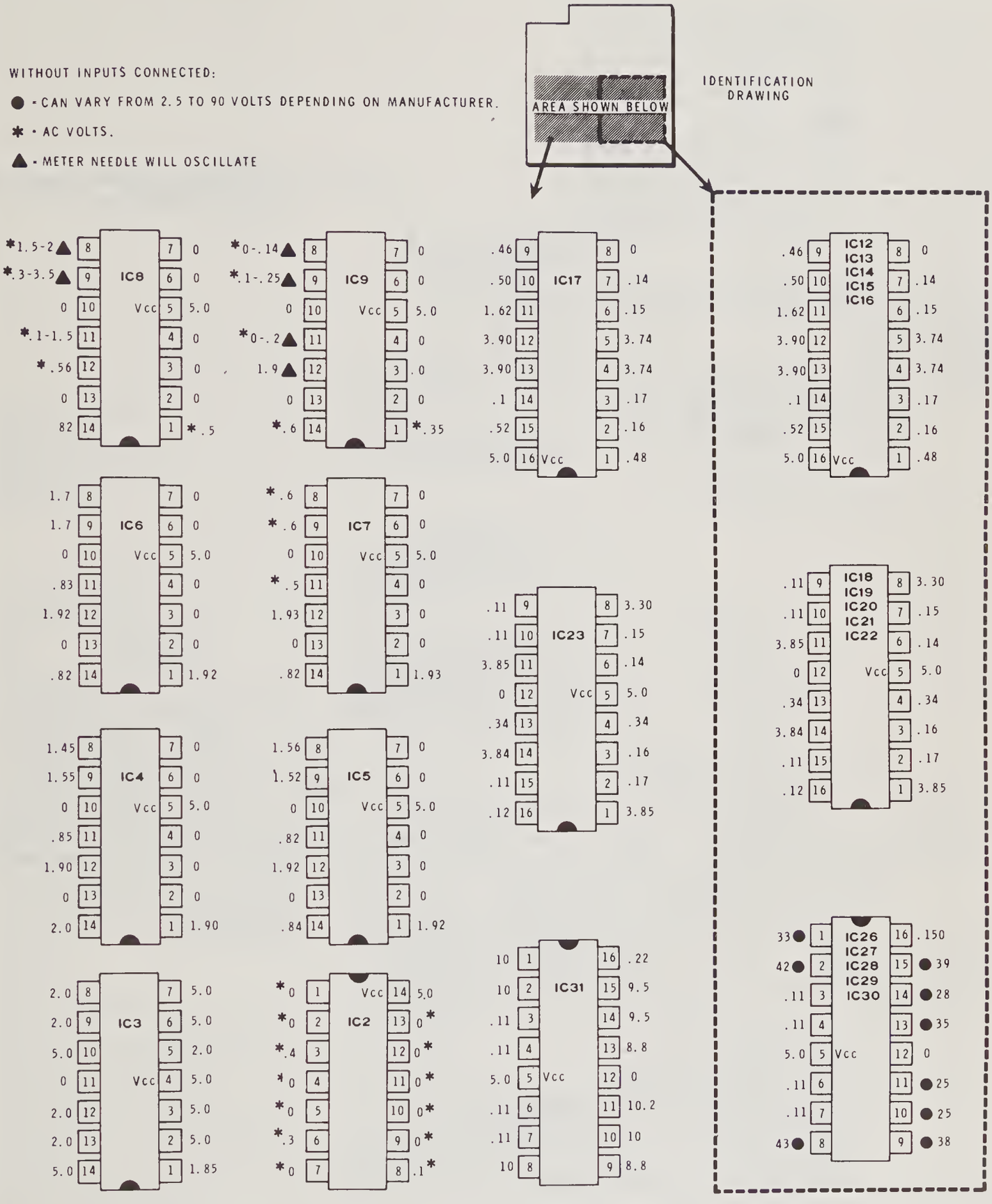
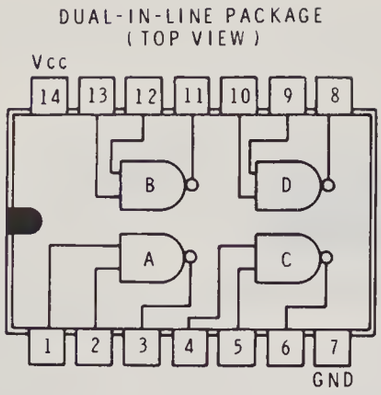


Fig. 7-20. Voltage chart for



Courtesy, Heath Co.

schematic in Fig. 7-3.



LOGIC LEVEL VOLTAGES

	MINIMUM	TYPICAL	MAXIMUM
GATE INPUT-HIGH	2V		
GATE INPUT-LOW			0.8V
GATE OUTPUT HIGH	2.4V	3.3V	
GATE OUTPUT-LOW		.22V	0.4V

IC2, 10, 11, 24, 32, 33, 34, 35
SN7400N, SN74H00N

TRUTH TABLE
(EACH GATE)

INPUTS		OUTPUT
A	B	
0	0	1
0	1	1
1	0	1
1	1	0

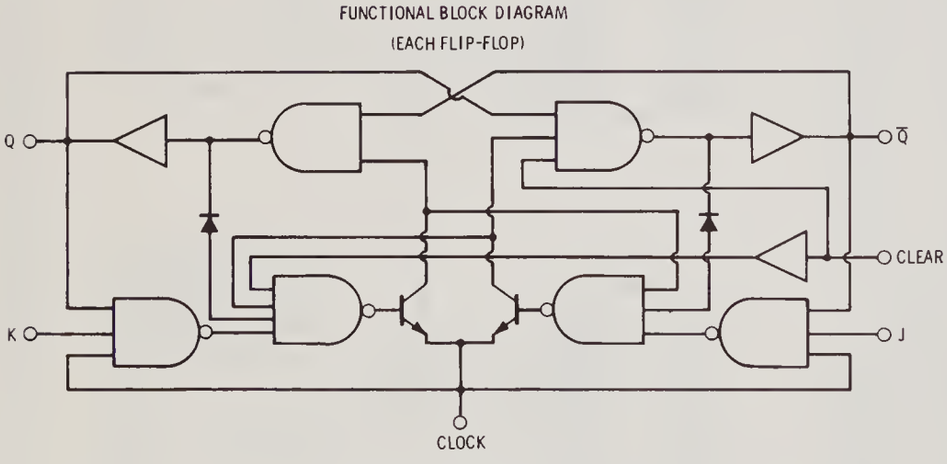
Courtesy, Heath Co.

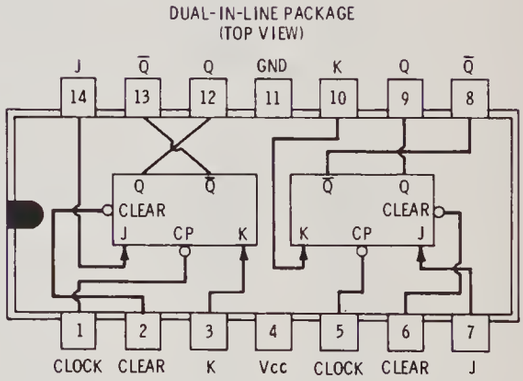
Fig. 7-21. IC arrangement, logic-level voltages, and truth table for NAND gates.

TRUTH TABEL

t_n		t_n+1
J	K	Q
0	0	Q_n
0	1	0
1	0	1
1	1	$\overline{Q}_n$

NOTES: 1. t_n = BIT TIME BEFORE CLOCK PULSE
2. t_n+1 = BIT TIME AFTER CLOCK PULSE





LOGIC LEVEL VOLTAGES

	MINIMUM	TYPICAL	MAXIMUM
INPUT-HIGH	2 V		
INPUT-LOW			0.8 V
OUTPUT-HIGH	2.4 V	3.2 V	
OUTPUT-LOW		0.25 V	0.4 V

IC25
SN74H103N

Courtesy, Heath Co.

Fig. 7-22. Truth table, IC arrangement, block diagram, and logic-level voltages for flip-flops.

Index

DIGITAL EQUIPMENT SERVICING GUIDE

This book has been written primarily for the technician whose troubleshooting experience has been limited to linear electronic circuitry, such as radio and television receivers. The principle difference between linear circuits and digital circuits is that the latter must be regarded in terms of switching circuitry. In other words, a digital circuit is either in the "on" state or the "off" state. In order to efficiently service digital equipment, the technican should be able to recognize the symptoms of a malfunctioning digital circuit. Since almost all types of electronic equipment will eventually use some digital circuits, the modern electronic technician must become familiar with these circuits.

The first chapter discusses basic digital circuits including flip-flops, gates, and pulse generators. Binary counters and shift registers are also covered in this chapter. Digital logic gates are explained in Chapter 2. The third chapter discusses binary adders, subtracters, and bcd counters. The different types of logic used in digital circuits are covered in Chapter 4. The various types of display devices and their operation are discussed in Chapter 5. The digital logic circuits used in electronic instruments are covered in Chapter 6 and the last chapter is devoted to digital frequency display equipment.

Binary arithmetic is introduced to the extent required for practical servicing of digital logic circuits. Terms that are unique to digital circuits are carefully explained throughout the book. Specialized digital test equipment such as logic probes, pulser, and logic clips are also discussed.

Bob Middleton is one of the few full-time professional free-lance technical writers in the electronics field. Since his many book and magazine articles are based on his own practical experience, they have proved invaluable to students, technicians, and engineers. His own workshop includes a wide variety of test instruments and other electronic equipment which he uses to prepare his many books.

Other SAMS books by Mr. Middleton include: *Computers and Artificial Intelligence, Record Changer Servicing Guide, Transistor TV Training Course, Color-TV Waveform Analysis, 101 Ways to Use Your Oscilloscope, Color-TV Servicing Guide, Know Your Signal Generators, Know Your Square-Wave and Pulse Generators,* and *Hi-Fi Stereo Servicing Guide.*

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